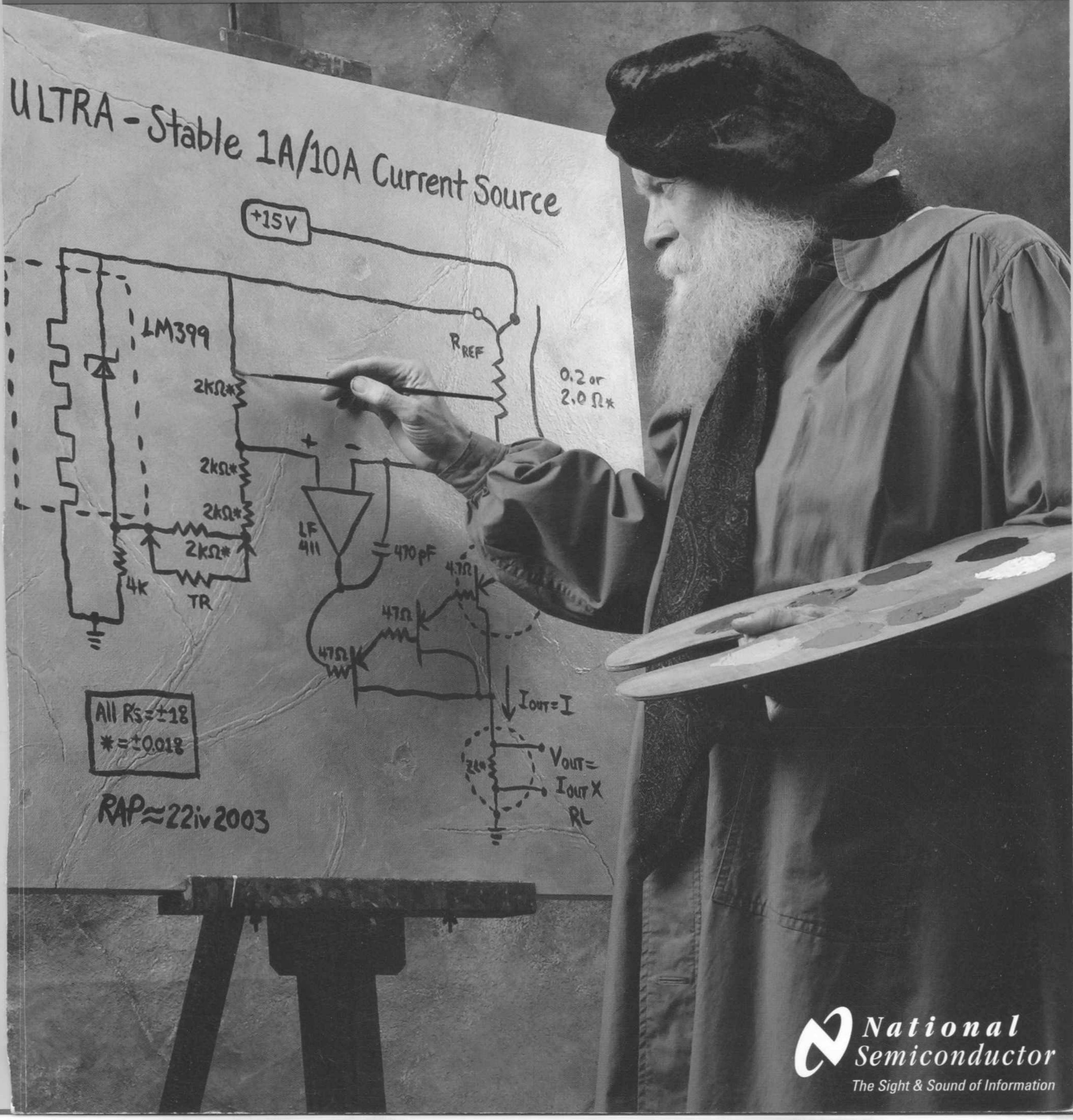
The art of analog design

Analog seminar series 2003/04



National Semiconductor
The Sight & Sound of Information

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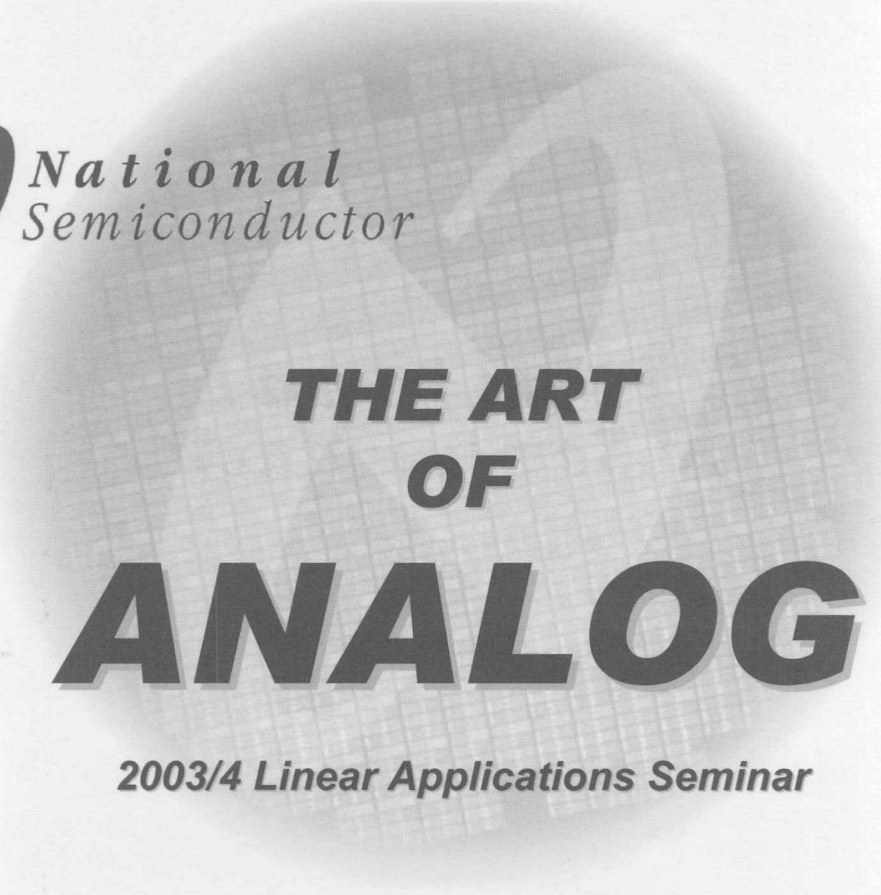
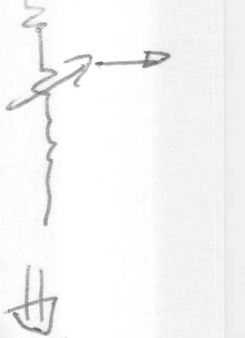


THE ART OF ANALOG

2003/4 Linear Applications Seminar



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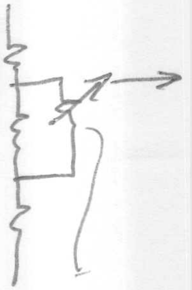

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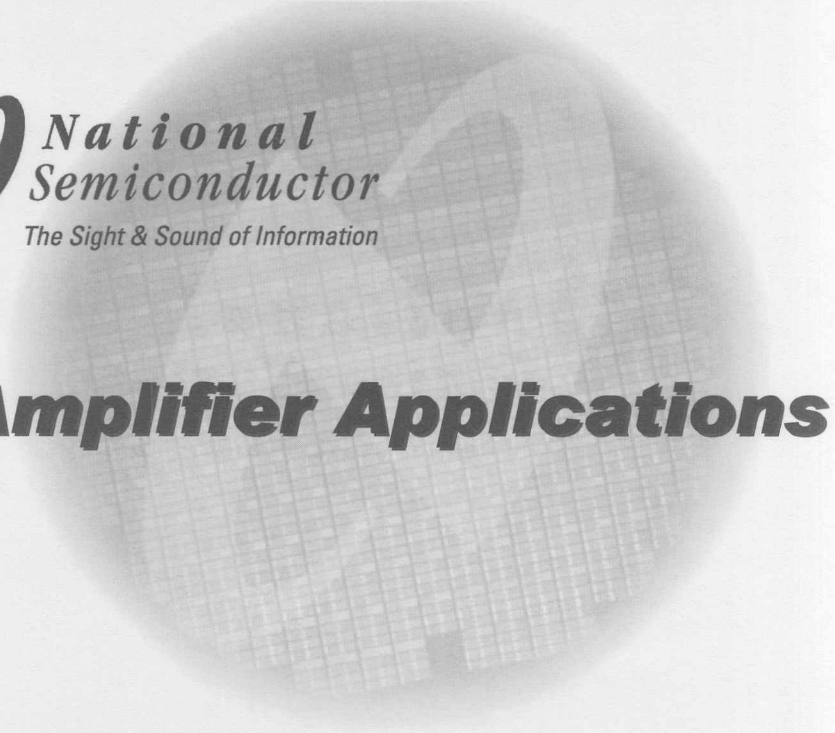

Amplifier Applications

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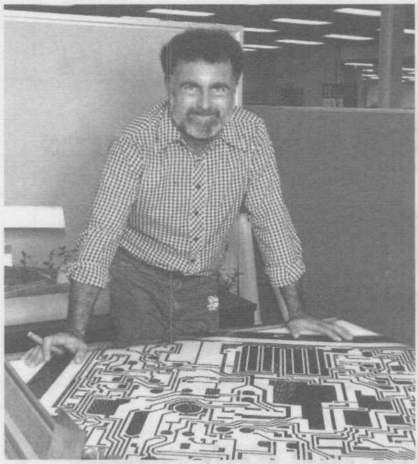
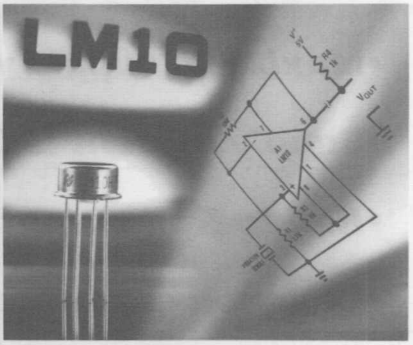
Low-Voltage, Low-Power Amplifiers



Robert Widlar (say wide-lar)



Bob Widlar's LM10:

1.2 Volt operation (in1978!)

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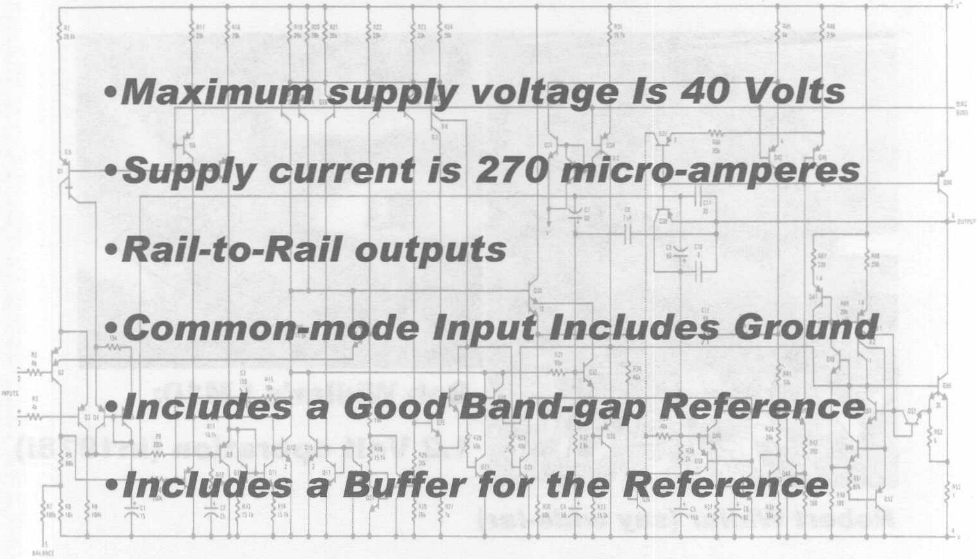
Low-Voltage low-power amplifiers have a rich tradition at National Semiconductor. More than 20 years ago Bob Widlar designed the LM10. This amplifier will work down to 1.1 volts, making it the lowest voltage amplifier we make today. Bob was an iconoclastic genius and contributed to many great designs at National. Today we are continuing his legacy by making entire classes of products that work at low voltages—below 5 volts and approaching 1 volt. Low-power amplifiers are another National specialty with several amplifiers in the portfolio that draw a few microwatts of power. Still other amplifiers draw more power in order to get the speed needed (a fundamental tradeoff) but these amplifiers have a shutdown function so they can be disabled when they are not being used, allowing overall system power savings.

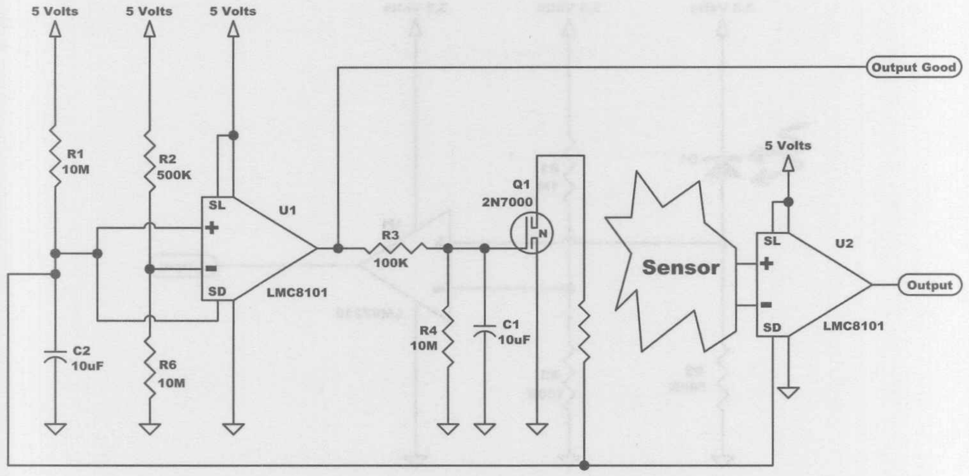
Lowest Voltage Amplifier National Makes Today.



- **Maximum supply voltage Is 40 Volts**
- **Supply current is 270 micro-amperes**
- **Rail-to-Rail outputs**
- **Common-mode Input Includes Ground**
- **Includes a Good Band-gap Reference**
- **Includes a Buffer for the Reference**

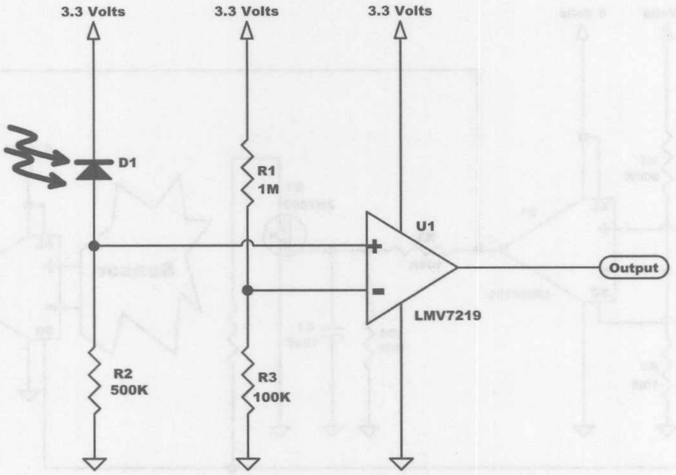
In order to appreciate what a great designer Bob Widlar was, we can review some of the specs of his LM10. First, and most remarkable, it is still the lowest voltage amplifier we make, working down to 1.1 volts. Equally astonishing, the part also will work with a supply as high as 40 volts. This allows the part to be used in older industrial systems that have +/- 15 volts supplies. The supply current is 270 microamperes. Anything under a milliampere is considered low-power. A part operating on 1.1 volts with a conventional output structure would have essentially no swing since each output transistor needs 0.6 volts for the base-emitter drop so Bob equipped the part with a rail-to-rail output stage so that the outputs can get to 20 millivolts of the rails. The part does not have rail-to-rail inputs, however the inputs can go all the way to ground much like the classic LM324 amplifier. In order to provide a full-service analog building bock, the part has a decent 200 mV band-gap reference as well as a buffer amp for the reference.

A micro micro micro Power Sensor Amplifier



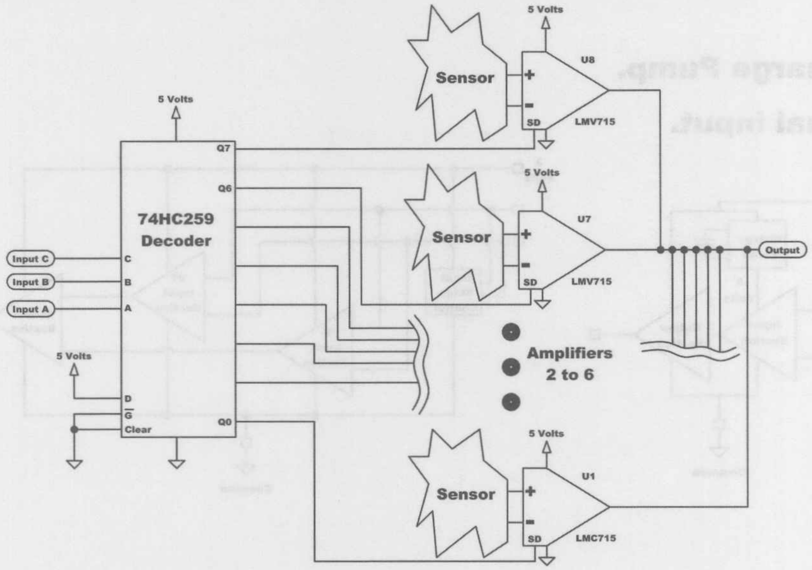
This circuit uses an amplifier that draws a little more current than some we make. It achieves its low power consumption by using the shutdown function of the amplifier to only enable the circuit for a relatively small time before going back to "sleep" R1 slowly charges C2 with a time constant of 100 seconds. Since the "SL" pin is strapped high, the shutdown pin turns on 1.5 volts below the top rail, or at 3.5 volts. Both the timing and the sensor amplifier turn on at this time. The U1 amp output is low and remains so until C2 charges to within 5% of the top rail by virtue of the 10M/500K set-point created by R2 and R6. At this time amp U1 switches high. R3 limits the charging current into C1 and slows the response down a little. Q1 turns on as C1 is charged up past the MOSFET's threshold voltage of 2.1 volts. Since the FET switches in the 1M resistor across C2 the timing amp, U1 has enough time to fully charge C1 to 5 volts. This charge is held on the gate of Q1 even as the voltage on the shutdown pin drops below the hysteresis level inherent in the part's design. As both parts are put into shutdown the output of U1 goes high-impedance. Because the FET must turn off for C2 to charge back up again, there is a bleed resistor R4 that slowly dissipates the charge on C1, creating another long time-constant that keeps the circuit in low-power mode. After Q1 is sufficiently turned off, C2 can begin charging up again, repeating the process.

Photodiode Comparator Application



This application uses a low-power comparator, the LMV7219, to sense the output of a photodiode amplifier. Infra-red light falls on the photodiode D1, generating reverse bias current. The R1/R3 ladder creates a 0.3 volts reference level at the inverting input. Consequently, when the photodiode reverse current reaches 0.6 microamperes the comparator switches. The fundamental limitation of this circuit relative to the other photodiode amplifiers in this seminar is speed. Since the photodiode is not looking into a virtual ground the voltage across it is changing as the photo-current changes across R2. The capacitance of the photodiode fights this changing voltage and limits the speed the circuit can toggle at. This simple circuit can be useful when there is a controlled IR source and speeds are under 1MHz. The 1.1 milliampere supply current of the LMV7219 is fairly low especially in view of the 7 nanosecond propagation delay but may be too high for battery powered circuits. Other lower-power, lower-speed comparators could be substituted.

A Bus-output Measurement System



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Amplifiers with shutdown functions can be bussed together and a particular amplifier can be invoked with a digital command. Insure the amplifier has tri-state outputs like the LMV715. The LMV712 has a shutdown function but the output is driven to the bottom rail (usually ground) when in shutdown mode. A serial to parallel chip can be used or in this case, a '259 latched decoder run in a mode that does not use the latch function. Since the output of this decoder is a high level, unlike the HC138, it can directly connect to the amplifiers, saving an inverter chip. Remember that there will be a finite time for the output of the amplifier to become valid depending on the circuit and worse case slew considerations, how far the amplifier has to slew before the loop closes and the output is valid.

New Low-Voltage Low-Power Amplifiers

Bipolar Input

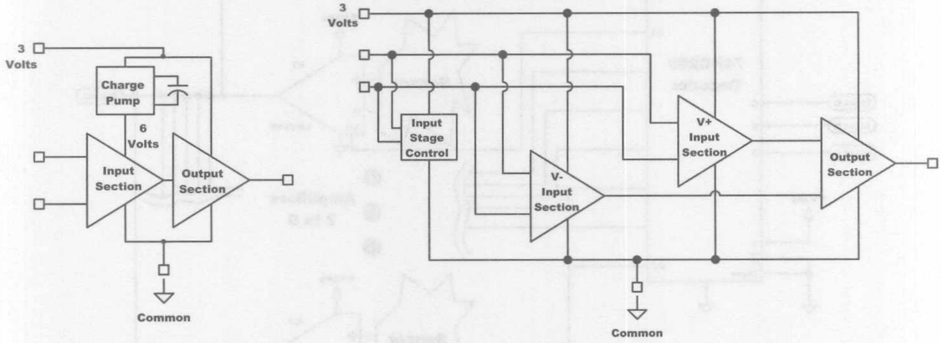
LMV321/358/324	*2.7V Low Power*
LPV321/358/324	*10uA Low Power*
LMV821/822/824	*High Performance*
LMV721/722	*Low Noise*
LMV931/932/934	*1.8V R-to-R I/O*
LMV981/982	*1.8V R-to-R I/O W/SD*
LM8261/8262	*2.5V, R-to-R I/O High Output Current Drive*

CMOS Input

LMV771/774	*1mV Precision*
LMV301	*1.8V Single*
LMC8101	*2.7V R-to-R I/O W/SD in micro SMD*
LMV341/342/344	*2.7V 100uA R-to-R O W/SD*
LMV710/711/715	*1.8V R-to-R I/O W/SD High Output Current Drive*
LMV712	*Dual Version of LMV711 with Independent SD*
LMV751	*7nV/rtHz Low Noise*

Rail-to-Rail Input Architecture

- **Charge Pump.**
- **Dual input.**



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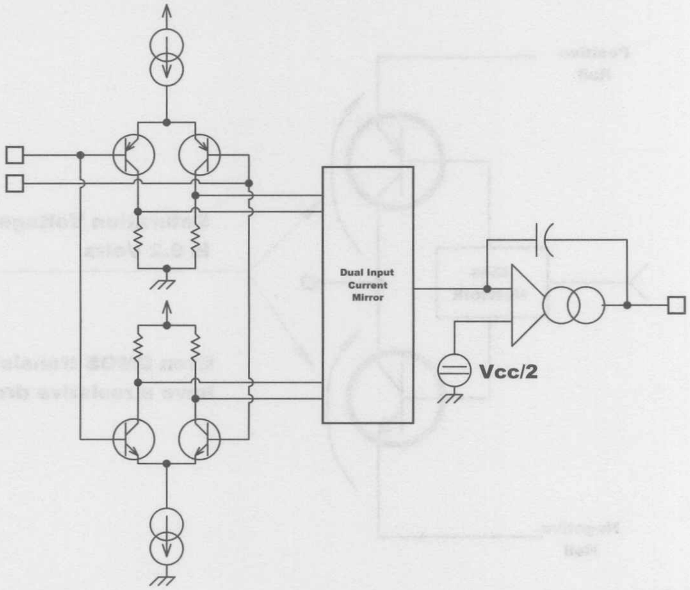
Low voltage amplifiers are often made with rail-to-rail input stages. These stages allow the inputs to work as long as they are kept within the supply rails. There are two fundamental ways to achieve rail-to-rail inputs in an amplifier. The first is to add an internal charge-pump circuit to the part such as shown in the left figure. The currents are low enough on the first stage that the charge pump capacitor can be internal. The charge pump doubles the supply voltage. This allows the use of a conventional PNP input stage like the ubiquitous LM324 uses. This stage is always good to the bottom rail. By powering it from split supply voltage the PNP bases can also be brought to the top rail. The disadvantage to this type of rail-to-rail architecture is that the switching noise of the charge pump may appear at the output of the part. The switching inside the charge pump also consumes power that will increase the supply current.

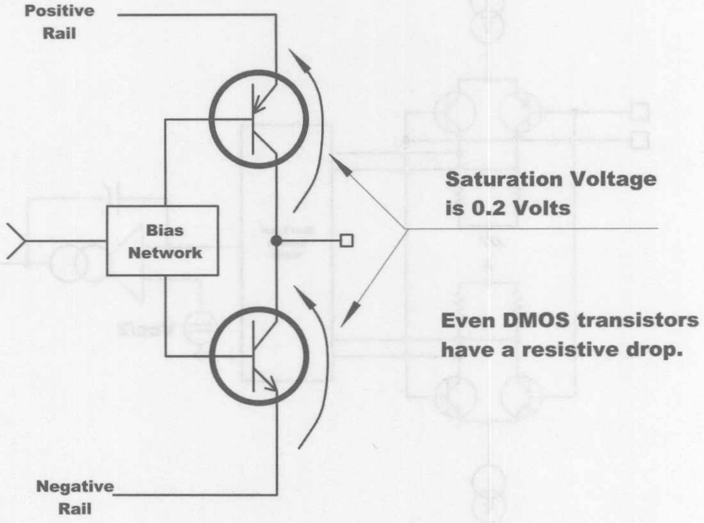
The second type of rail-to-rail input stage uses a dual input stage. One of the stages can work down to the bottom rail (the PNP stage) and one can work to the top rail (the NPN stage). There needs to be a control stage that smoothly switches the stages as the signal gets close the rail. In general the PNP stage is used for input voltages close to the bottom rail all the way up to about a volt below the top rail. The control section transitions the active input to the NPN stage so the input signals can go to the top rail. The inputs can often go a little beyond the rail, to almost a diode-drop. This means the inputs of a rail-to-rail input stage with this architecture can go from a half-volt below the bottom rail to a half volt above the top rail. The reason the transition is not at the mid-point between the rails is because the stages do have different offsets and other parameters and many operational amplifiers are used with small signals right at half-supply. By having the transition between the stages be a volt below the top rail, the part has consistent parametrics around mid-supply.

Rail-to-Rail...Input Stage



This is a detailed view of a representative rail-to-rail input stage of the dual input type. One can see that one stage uses a pair of differential PNP transistors and the other uses differential NPN transistors. It is important to note that this type of amplifier has two different sets of input parameters depending on which differential pair is active. As explained earlier, the usual setup is for the PNP pair to do the work until the common-mode voltage gets to about 1 volt below the upper supply rail. Then control is passed to the NPN stage, which operates the rest of the way to the upper rail. Since there are two different differential pairs it should be obvious that there will be two different offset voltages for the amplifier, depending on the common mode value of the input pins. Small signal bandwidth and other AC parameters are also different for the two. If the amplifier is used to buffer an input to an A-to-D converter one must be aware of the offset error change as the part transitions between input stages.

Rail-to-Rail...Output Stage



Saturation Voltage is 0.2 Volts

Even DMOS transistors have a resistive drop.

Conventional output stages have a voltage-follower totem pole output, with an NPN transistor on top and a PNP on the bottom. The problem with this is that even if the internal circuits in the amplifier could bring the bases of these output transistors to the supply rail, the V_{BE} diode drop from the base to the output means that the output can never be driven closer then 0.6 volts to either rail. By flipping the transistors around, as Bob Widlar did in the LM10 in 1978, the base drive problem goes away. The bias network becomes far more complicated but that is inside the part and National's problem, not yours. If you remember your transistor physics you may know that the saturation voltage (the maximum "on" condition) of a transistor is about 0.2 volts. This means that a rail-to-rail output still can never really reach the rails. It can get even closer then 0.2 volts when using DMOS FET transistors, since they are resistive in the on state, but even then, as soon as you draw current out of the part, the a voltage drop will be created that pulls the output away from the rail. A special problem should be noted at this juncture. If the rail-to-rail input is actually at either rail and the part is configured as a voltage follower, the output will never be able to reach the rail.. This means that the feedback loop stops working and the amplifier does everything it can to try and bring the output even closer to the rail. "Doing everything it can" means that the amplifier will start shoveling base current drive into the associated output transistor. Most amplifiers are designed with clamp circuits around this base drive so that base current does not become excessive but you can see from the diagram that this base current is not delivered to the load like with a voltage follower stage. It is sourced or sunk into the respective rail. One should be aware that when a part is driven so hard that the loop can't close, the supply current will go up until that base-clamp circuits kicks in. This might explain why your micro-amp class amplifier is sucking up a few milliamperes when the output bangs against either rail.

Rail-to-Rail Outputs...Definition

So can a rail-to-rail output REALLY ever reach the rail?

Does this mean semiconductor companies are all a bunch of liars?

(Hint: Marketing people are involved.)

Definition: Rail-to-Rail outputs simply means closer than 0.6 volts (and that's all it means)

Now that we've explained that rail-to-rail outputs really can't reach the rail you might wonder why they are called rail-to-rail and not close-to-the-rail amplifiers. Well, the marketing people got involved that's why. And not National's marketing people. The entire industry has adopted this nomenclature. You have to admit that "rail-to-rail" sounds a lot better then "close-to-the-rail". And the performance implied by rail-to-rail is not necessarily the same either, as we noted with the DMOS versus bipolar output transistor issue. So what does rail-to-rail mean? All that can be said generically is that "rail-to-rail" means that the outputs can get closer then 0.6 volts to the rails. Sometimes it can get a lot closer but it can never reach the rail. And remember, just because the inputs may work when they are a half-volt past the rail, there is no magic that can make the outputs get past the rail. (Unless you add a pull-up resistor! Cheater!)

Who Really Needs Rail-to-Rail Inputs?

- *You rarely need a rail-to-rail input amplifier*

What is the fundamental application where you do?

- ***The Buffer***

Our applications manager has a valid conjecture concerning rail-to-rail input amplifiers. His conjecture is that: "Rail-to-rail inputs are rarely needed". Think about a system with any appreciable gain, say, a gain of two. Well, the inputs will only have to go one-half the excursion of the rail-to-rail voltage in order to drive the outputs all the way to the rail. And any inverting amplifier has the input pins biased up at one place, usually mid-supply, and certainly won't need the inputs to go anywhere near either rail. Remember, there are many amplifiers that can work to either the positive or negative rail. If you wanted to sense current high-side or low-side you could use one of these with no problem. In fact there is only one application that can really take advantage of the rail-to-rail input: The non-inverting voltage follower, also known as a buffer. Here the plus pin (and the minus pin if the amplifier is working) will be swept across the entire range of supply voltages. This is most commonly used when needing a low impedance input to an A to D converter or when buffering a DAC to give an output that can swing from rail to rail.

Things That Can Go Wrong

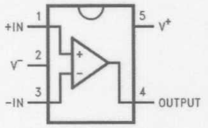
- **Different pin-outs**
- **Power supply sequencing**
  - **Latch up**
  - **Power through ESD diode**
  - **Slow power-up or power-down**
- **Temperature issues**

Every designer wants to know the "gotchas" of designing with a given parts family. As most of us have learned, analog design is full of "gotchas". Low-power, low-voltage parts have their own peculiarities. One of the most basic is that there are different pin-outs for the small packages such as SC70 and SOT23. The proliferation of micro SMD (solder-bump) packages will only make this worse. Another headache is the sequencing of the power supply, how the power is applied relative to the input signals. A final concern is temperature. We'll assume you know the issues of high temperatures, especially with theses tiny packages that can not dissipate anywhere near the power of a DIP or SO package. There are also problems that can occur at cold temperature. Stability suffers and the common-mode range or output drive can suffer. The following few slides details these problems and explains what National is doing to help you.

Watch Those Pin-Outs!

There are FOUR SC70/SOT23 pin-outs possible.

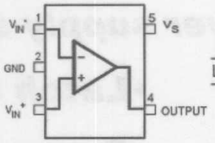
5-Pin SC70-5/SOT23-5



LMV331M7
LMV331M7X
LMV331M5
LMV331M5X

Top View

SOT23-5

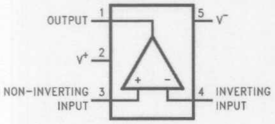


LM397MF
LM397MFX

Same as TL331!

Top View

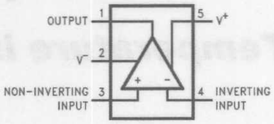
5-Pin SOT23-5



LMC7101AIM5
LMC7101AIM5X
LMC7101BIM5
LMC7101BIM5X

Top View

5-Pin SOT23



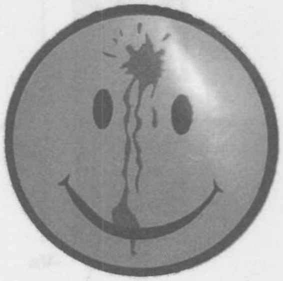
LM7121IM
LM7121IMX
LM7121IM5
LM7121IM5X

Top View

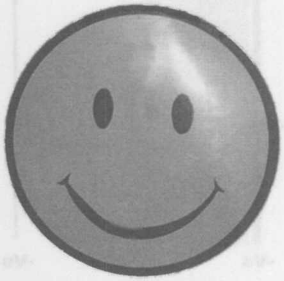
Since low-power and low-voltage amplifiers are often used in handheld applications, these amplifiers are offered in very small packages. SOT23 and SC70 are two common package sizes used by many manufactures. Unlike DIPs and the SO8 package, there is no standard pin-out for the SOT23 and SC70. This can make selecting substitutions for existing applications difficult. This slide shows the 4 different pin-outs National uses. Note the two parts on the bottom of the page have seemingly identical pin-outs until you notice that the power pins are reversed. Also note that Texas Instruments has a part called the TL331 that is in a different pin-out then National's LMV331. The TI part is a comparator; the National part is an amplifier. All this means you have to be very careful when substituting parts intended for an SOT23 or SC70 package. Having the same specs is not sufficient, you have to insure the pin-outs are the same. There is an equally diverse set of pin-outs possible in the micro-SMD package. What's worse is that the footprint for these die-size packages may be different—the center-to-center distances between the solder bumps is a function of the die layout, not any formal industry standard.

Power Supply Sequencing

- **Latch-up**
- **Power delivery through ESD diode**
- **Unstable/unpredictable outputs on power-up or power-down**

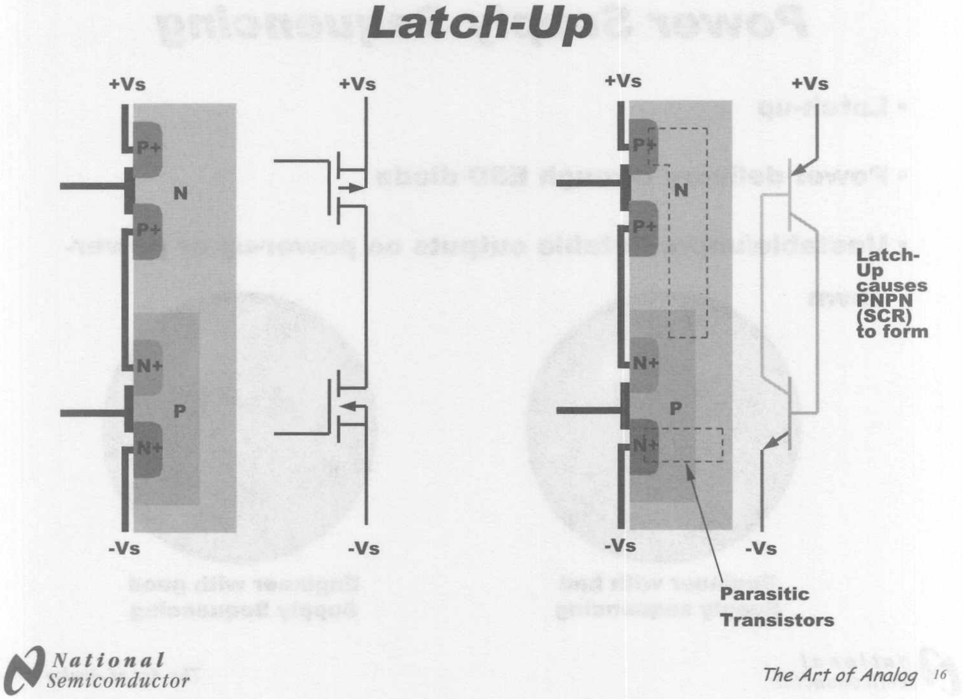


Engineer with bad Supply sequencing



Engineer with good Supply Sequencing

As power conservation becomes more and more important many electronic systems utilize power management schemes that turn off various sections of the circuitry until they are needed. This is reasserting the need to understand power supply sequencing issues. In general it is desirable to first make sure the part has a suitable ground, then apply power to the part, and then activate the input circuitry that presents voltage to the input pins. Now the ground side is usually pretty easy, most times it can just be left connected. Applying power is straightforward too, although sometimes applying the power too fast or too slow can cause problems. The real headache is often insuring that there is no voltage on the input pins until after power is applied. There are three common consequences of having energy on the inputs when power is applied to the amplifier. Latch up is primarily an issue with CMOS amplifiers. The other two, power delivery through the ESD diode and unstable outputs, can plague any type of amplifier.



Latch-Up

Latch-Up causes PNPN (SCR) to form

Parasitic Transistors

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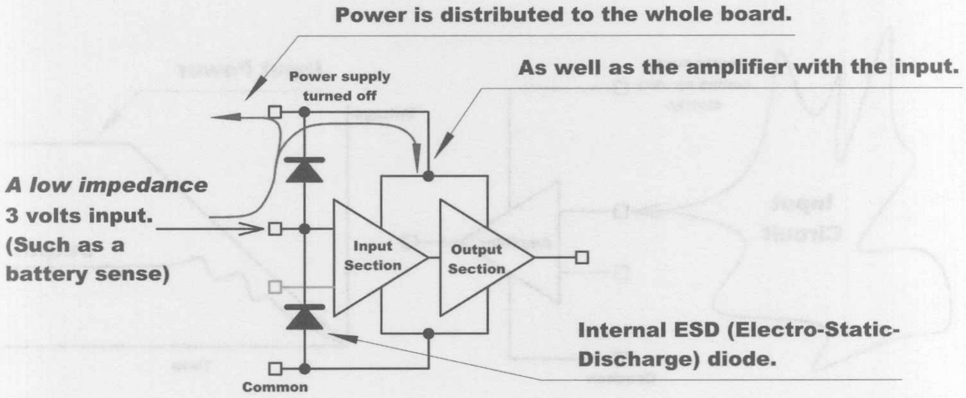
The Art of Analog 16

Latch up occurs when the P-N junctions between transistors and the die substrate they are laid out on create a parasitic SCR device. As you may remember, SCRs are four layer (PNPN) devices that once triggered, stay on until power is removed. You can see from the diagram of the interconnected PNP and NPN transistor above that once any current begins flowing in the base of either transistor the current will self generate and latch the structure "on". The current usually stops when the bond-wire melts or the part explodes. This is primarily a problem in CMOS parts. Bipolar parts rarely exhibit latch up and dielectrically isolated processes that put each transistor into their own little glass tub (such as our VIP10 process) also are impervious to latch up. If you can limit the current into the input pin you may be able to prevent latch up with CMOS parts. Try putting a high-value resistor in series with each input pin. Be sure to evaluate the circuit over temperature and supply variations as well as supply turn-on speed to insure that latch up won't occur. You can also limit the current into the power supply pin but that will not prevent the latch-up, it will only save the part from destruction. In order to get the part to work, power will have to be removed from the supply pins and the inputs and then the part turned on again.

Power Delivery Through ESD Diode



Power is distributed to the whole board.

As well as the amplifier with the input.

A low impedance
3 volts input.
(Such as a
battery sense)

Internal ESD (Electro-Static-Discharge) diode.

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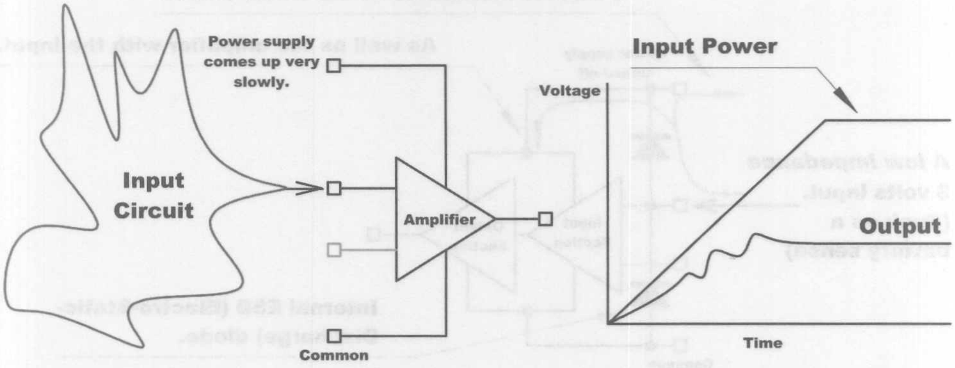
This slide shows a problem that can affect any amplifier from any manufacturer. All modern amplifiers have a pair of ESD (Electro-Static Discharge) diodes on every pin. These diodes protect the delicate internal circuitry of the part from static discharges in handling and assembly. If the discharge is positive into the input pin shown, the high side diode conducts the energy to the positive rail and if the discharge is negative the low-side ESD diode is forward biased and clamps the input pin to the bottom rail. In this fashion all the pins are clamped to values no further than 0.6 volts from the supply pins. Looking at the diagram above one can see that having a low-impedance voltage on one of the input pins when power is turned off to the amplifier is sure to cause problems. The ESD diode on the input pin will conduct and the input will be connected to the supply pin by a diode drop. That is why it is low impedance inputs that cause a problem. If there were a meg-ohm resistor hooked to the pin, there would be enough to current available to forward bias the ESD diode but 3 micro-amperes of current isn't going to power up very much of anything. Now imagine that some input is directly connected to a battery. That low impedance source can deliver plenty of current. Enough current to forward bias the diode and then flow into the entire power node of the board, powering up the whole system. If enough current flows (100 milliamperes or so), the ESD diode will melt and short out, ruining the part. As with latch-up, the solution is to add series resistance to the input pins to insure that the there is not enough current available to power the system through the ESD diode. The ESD diode can take tens of milliamperes of current but it is usually more of a problem that current is being wasted. If at all possible, try to insure that everything in the circuit, power as well as inputs, are disabled by the power management scheme. If something is drawing power you can't explain, this is a good place to look first.

Unstable / Unpredictable Outputs on Power-up or Power-down



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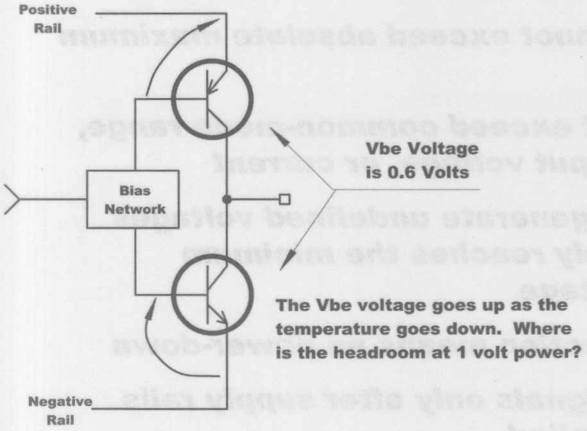
The above slide shows the problems that can occur if the power comes up too slow in a system. When amplifiers are below their specified voltage there is no guarantee what the outputs will be doing. Very often the outputs will oscillate mildly or bang into the rails until the amplifier reaches some minimal voltage. If this output is hooked to something critical, that critical function won't be stable until the power is established above the minimum need by the amplifier. You may make the best slitter-degutter in the entire cattle industry, but please insure it doesn't start slitting and degutting until it is supposed to. It should be noted here that supplies that come up too fast can sometimes cause problems. The fast rise-time may couple to the output and cause a problematic glitch. In all cases be sure the amplifier is tested in a system that uses the same power system as in production. There are many stories of disasters that occurred because the analog system was developed and tested with laboratory power supplies and then things go very wrong when they are hooked to a noisy soft-starting switcher in the real product.

Temperature Issues

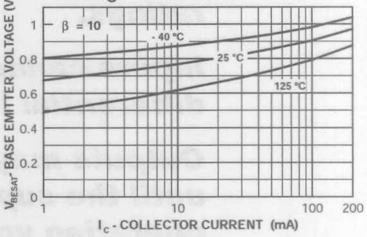
- **Watch those low temperatures**



Vbe Voltage is 0.6 Volts

The Vbe voltage goes up as the temperature goes down. Where is the headroom at 1 volt power?

Base-Emitter Saturation Voltage vs Collector Current



Most system-level designers regard high temperatures as the enemy. We all know that getting a part too hot will waste power, cause performance to suffer and ultimately, melt the part. You should also realize that semiconductor physics is not kind at cold temperatures either. With regards to transistor physics, one of the disturbing things that happens is the V_{BE} voltage goes up as the temperature goes down. If the V_{BE} of the transistors is 1 volt it's going to be pretty hard to design a part to work at a power supply voltage of 1.2 volts. There can also be stability issues at cold temperatures. Oscillations can form into moderately difficult (i.e. capacitive) loads that don't show up at room temperature. There is a reason the charts section of the datasheet has charts that deal with temperature effects. Be sure to test and evaluate the system at low temperatures as well as high.

Power Supply Sequencing Summary

- **Power supply sequencing:**
  - **VIP10 and Bipolar devices resist latch-up**
  - **Input pins cannot exceed absolute maximum ratings.**
  - **Inputs cannot exceed common-mode range, differential input voltage, or current**
  - **Outputs may generate undefined voltages until the supply reaches the minimum operating voltage**
  - **Shutdown function means no power-down**
  - **Apply input signals only after supply rails have been applied**

Most of you know National's web site sets the standard for the entire industry. Our manufacture of LAN chips spurred our early adoption of intranets and it only followed that our internet presence would be world-class. When sifting through product data the National web site can help you call up the information such as pin-outs and package options in a speedy and accurate way. Power supply sequencing issues can be ameliorated by our VIP10 process as well as our other bipolar processes. You can utilize our parts having the shutdown function to allow power to be present at the amplifier to minimize latch-up and ESD diode power delivery problems. We specify our low-voltage parts at several voltages that can indicate the stability of the output as the power supply comes up. We specify most of our parts at –40 degrees C which can assure you of the part's functionality at severe low temperatures.

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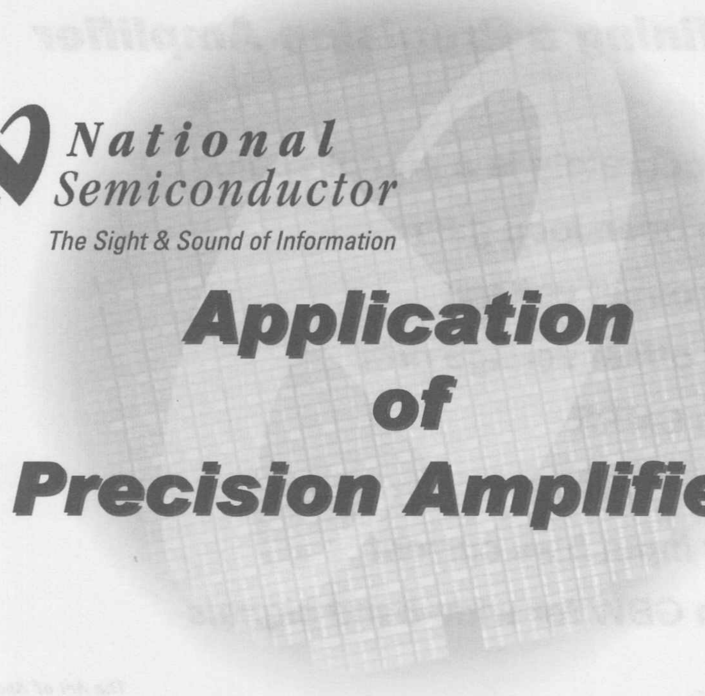
The Sight & Sound of Information



Application of Precision Amplifiers

Defining a Precision Amplifier

- How accurately is a signal scaled?
  - *High open loop gain*
  - *Low offset voltage*
  - *Low offset voltage drift*
  - *High CMRR*
  - *High PSRR*
  - *Low input bias current*
  - *High GBW for wide-band signals*

Precision amplifiers accurately process a signal while buffering, scaling or filtering it. In general, Precision has been interpreted as "good" DC specifications, such as low offset voltage, low offset drift, etc. Some applications will also require precision AC characteristics.

OP Amp Error Sources

$$e_{id} = \frac{e_O}{A_{VOL}} + V_{OS} + \left(I_{B+}\right)\left(R_{S+}\right) + \left(I_{B-}\right)\left(R_{S-}\right) + \frac{e_{CM}}{CMRR}$$

- **Major input referred error sources of an Op Amp**
  e_{id} = 0 for ideal Op Amp
- **Precision requires Error terms to be small relative to the signal being processed.**
- **Do not forget about frequency.**

This equation considers the major contributors to errors in op amps. The value "e_{id}" is the voltage between the two inputs of the op amp and is equal to zero if the op amp is ideal.

The first term, e_o/A_{VOL} , results from the finite gain of the amplifier. There must be a small differential voltage across the input to produce an output voltage. For example, if the output of an amplifier is 1.0 volts DC and the open loop gain is 100dB the error voltage across the inputs is $1/10^5 = 10\ \mu V$

The second term, input offset voltage or V_{OS} , is a result of small imbalances on the differential input stage of the amplifier. The input offset voltage is also multiplied by the noise gain of the amplifier with its feedback. At high gains the V_{OS} can become a large offset error.

The third and fourth terms result from the input bias currents in conjunction with any source resistance. Any current flowing into the amplifier's input will cause a voltage drop across the source resistance of (I_B x R_S) This has two effects. The first is to generate an apparent offset voltage at the input to the op amp if the equivalent source impedances on each input are not equal. The second is to add an error voltage to the signal that changes its apparent magnitude.

The last term brings in the effect of the common-mode voltage seen by the amplifier's input. The common mode voltage, e_{CM} , is defined as the average voltage on the amplifier's inputs, $(e_+ + e_-)/2$. For example, if the common mode voltage is 1 volt and the CMRR is 80db, the error on the amplifier's input due to the common mode voltage is $1/10^4 = 100\ \mu V$

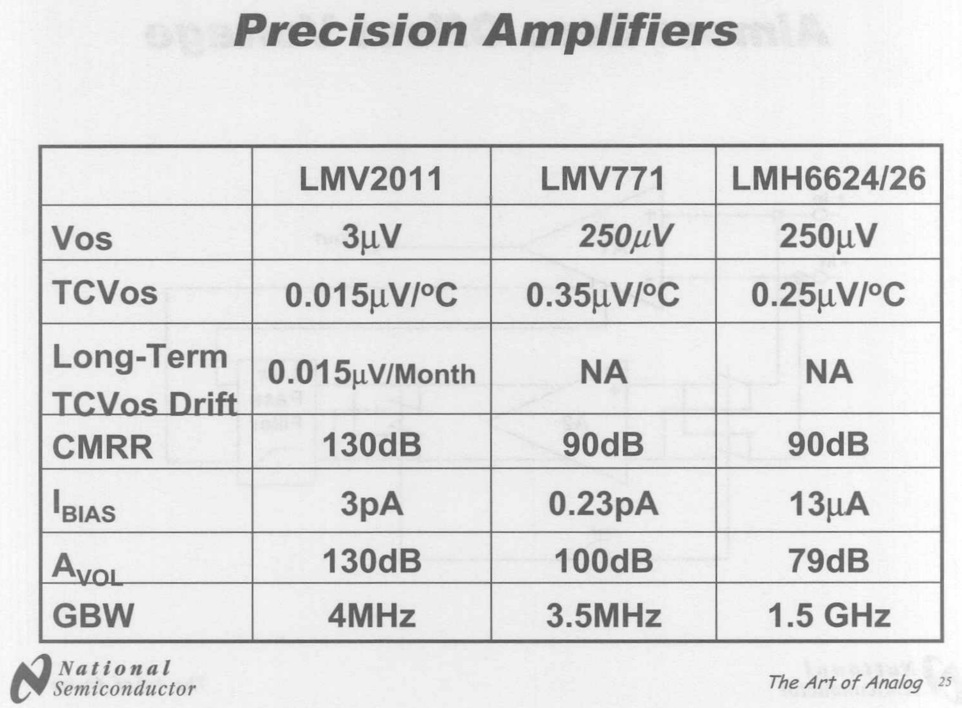
Each of the above error sources needs to evaluated with respect to the specifications of the amplifier being considered.

As the frequency of the signal increases the Open loop gain AVOL and the CMRR will roll off with increasing frequency.

Precision Op Amps

- **LMV2011**
  - *Chopper stabilized*
- **LMV771**
  - *Low offset, Low noise, High drive*
- **LMH6624/26**
  - *Low offset, 1.5 GHz GBW*

Three recent additions to National's precision amplifiers are the LMV2011, LMV771, and the LMH6624 and LMH6626.



Precision Amplifiers

	LMV2011	LMV771	LMH6624/26
Vos	3μV	*250μV*	250μV
TCVos	0.015μV/°C	0.35μV/°C	0.25μV/°C
Long-Term TCVos Drift	0.015μV/Month	NA	NA
CMRR	130dB	90dB	90dB
I_{BIAS}	3pA	0.23pA	13μA
A_{VOL}	130dB	100dB	79dB
GBW	4MHz	3.5MHz	1.5 GHz

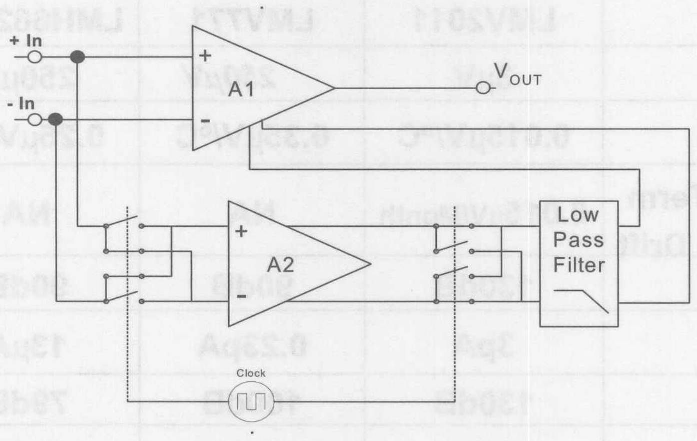
National Semiconductor

The Art of Analog 25

The LMV2011 is a MOS input chopper-stabilized amplifier offering near zero offset voltage and offset voltage drift. The LMV2011 is available in singles, dual (LMV2012) and quads (LMV2014). The LMV771 is a MOS input op amp which is designed to provide low offset voltage and low offset voltage drift and good output drive capability.

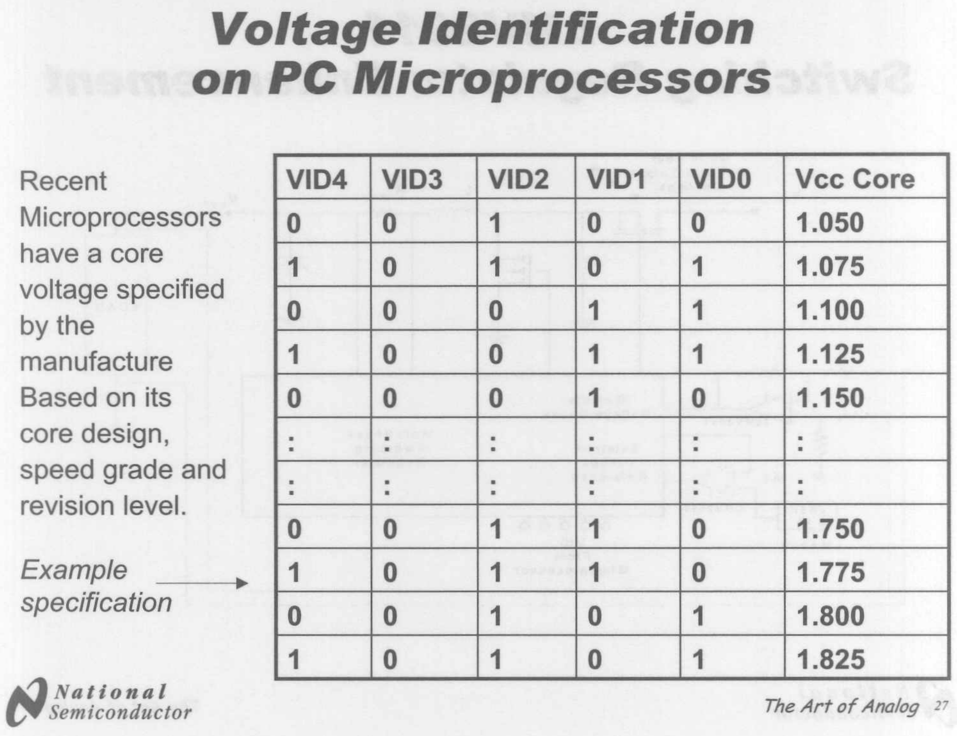
The LM6624 and LMH6626 are bipolar-input, laser-trimmed, low-noise, wide-bandwidth amplifiers that are available in singles and duals.

Almost Zero Offset Voltage



Chopper stabilized amplifiers have been available in various forms for many years. While they did remove most of the offset voltage, there was low frequency noise added to the signal of interest. The LMV2011 makes use of several patented topologies that eliminate any additional low frequency noise from the signal.

Referring to the block diagram of the LMV2011 above: The LMV2011 is a chopper stabilized amplifier which uses active input offset voltage compensation to achieve very low offset voltage and offset voltage drift. The amplifier A1 is the is the signal path amplifier while amplifier A2 is the offset correction amplifier. The input offset voltage of amplifier A1 is chopped into an AC signal by the switch arrangement at the input of A2. The The chopped offset voltage is amplified by A2 and de-chopped by the switch arrangement on the output of amplifier A2 and filtered by the lowpass filter. The filtered offset voltage correction signal is used to subtract the offset voltage present in A1.



Voltage Identification on PC Microprocessors

Recent Microprocessors have a core voltage specified by the manufacture Based on its core design, speed grade and revision level.

Example specification →

VID4	VID3	VID2	VID1	VID0	Vcc Core
0	0	1	0	0	1.050
1	0	1	0	1	1.075
0	0	0	1	1	1.100
1	0	0	1	1	1.125
0	0	0	1	0	1.150
:	:	:	:	:	:
:	:	:	:	:	:
0	0	1	1	0	1.750
1	0	1	1	0	1.775
0	0	1	0	1	1.800
1	0	1	0	1	1.825

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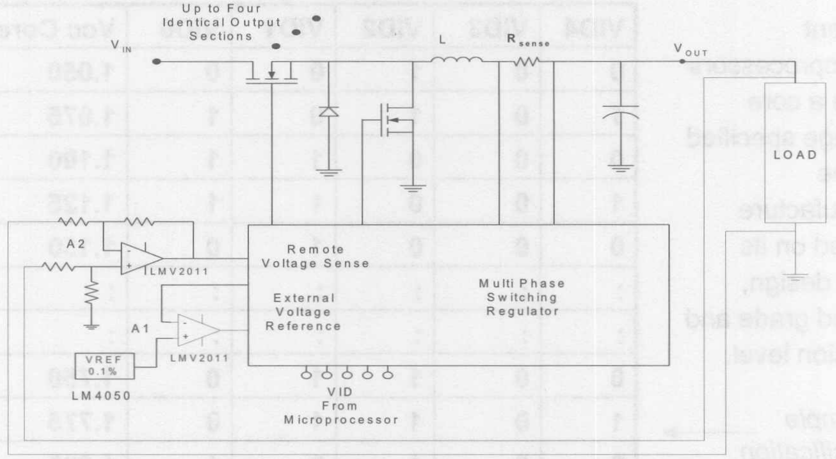
The Art of Analog 27

The x86 microprocessors from AMD and Intel use a group of five pins to define the operating supply voltage required by it. The group of five pins, known as the "Voltage Identification" or "VID" pins are used to set the voltage of the voltage regulator on the mother board. This allows the computer's motherboard to support several versions of the microprocessor. The range of adjustable voltages and resolutions with in the section range are determined by the requirements of a specific family of microprocessor. The table shown above shows an adjustment range of 0.775 volts, 1.050 to 1.825 volts, and a resolution of 0.025 volts. The current required by the microprocessor is in the range of 35 to 60 amps. The motherboard design for these microprocessors typically use a multiphase switching regulator on the motherboard with the voltage set by the VID pins from the microprocessor connected to the VID input pins on the switching regulator controller. Several of the features these chips have are remote sensing of the voltage output and on chip voltage reference with a reference voltage divider.

There are situations in which tighter tolerances of the output voltage are required, initially and over temperature. In other situations a different range of output voltages is desired. Many of the multiphase switching regulators available have pins that provide for an external remote sense amplifier and external voltage reference. These pins give the designer several additional degrees of freedom when designing the switching regulator.

LMV2011
Switching Regulator Enhancement



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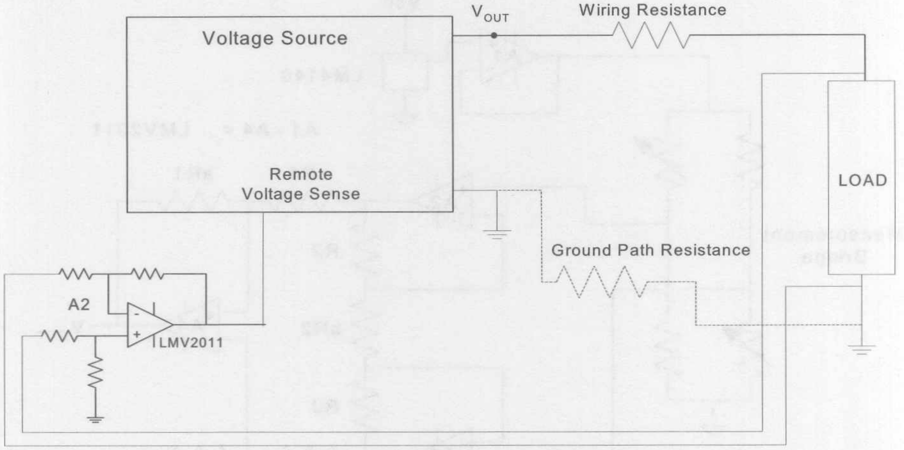
The Art of Analog 28

The microprocessor supply voltage tolerances have become key parameters in maintaining correct operation of the microprocessor, and there may be a requirement to regulate the output voltage to tighter tolerances. The tighter tolerances required may not be met by the voltage reference and remote sensing circuitry integrated on to the switching regulator controller. Most of the multiphase switching regulator controllers have pins that permit the use of external reference voltages and sense amplifiers.

In the circuit above the LMV2011, a chopper-stabilized amplifier, is used to provide a near-zero-drift remote-sense amplifier, error amplifier and a voltage reference. The voltage reference, LM4050, can be used to provide a higher quality reference or a different value of reference voltage. Amplifier A1 is being used as a zero drift error amplifier. The amplifier A2 is configured as a differential amplifier for feeding back the actual voltage at the at the load. Remote sensing compensates for the voltage drops in the wiring connecting the regulator's output to the load.The next slide has additional details.

A second use of the external amplifiers and voltage reference is to change the preset voltage range and resolution of the VID control pins. For example, the gain of the remote sense amplifier with a value different than 1 will scale the output voltage by the reciprocal of the gain. Likewise, the external voltage reference's value can be used to change the range and resolution of the output voltage.

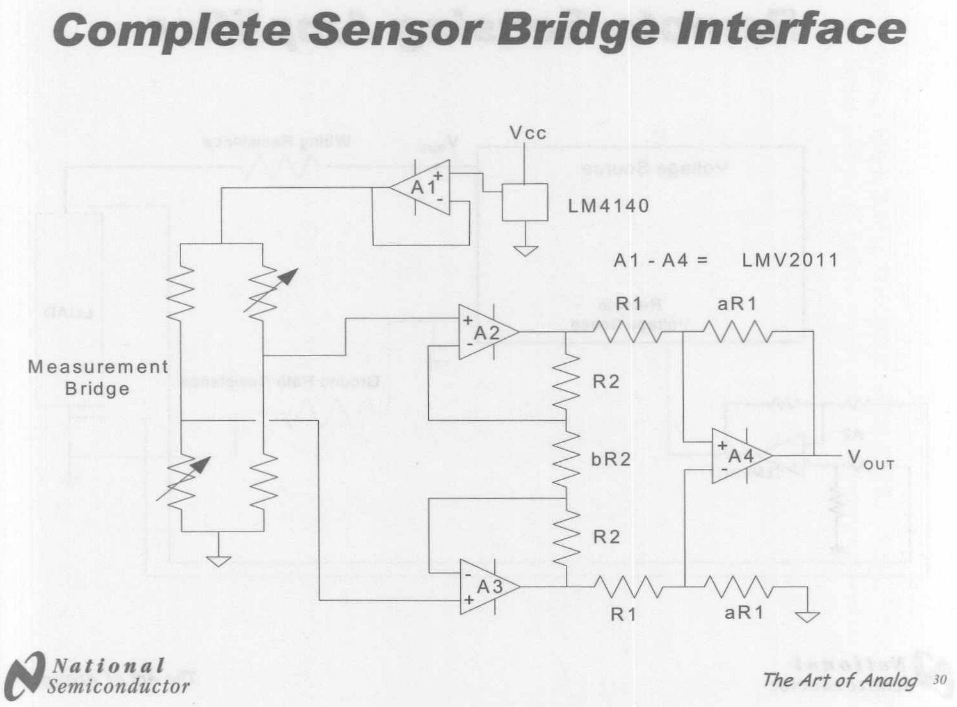
Remote Sensing Amplifier



There are measurement and control situations in which the voltage across a load, or the current through a load, must be controlled very precisely. For example, in the previous slide the voltage is programmed in 0.025 volt steps. Continuing with the the example from the previous slide.

The load is a P4 or Athlon microprocessor requiring a current of 50 amps. In the schematic above the connection from the power supply to the microprocessor has some resistance in the path from the power power supply and there is some resistance in the ground return path. If the combined resistance in these paths is a relatively small 0.001 Ohms the voltage drop in the paths is VDROP = 0.001 x 50 = 0.050 volts. This voltage error is twice the size of the required resolution of 0.025 volts. An additional error will result when the wiring is heated by the power dissipation in it.

To compensate for the wiring losses a remote sensing amplifier is used to measure (sense) the voltage directly at the load. In the above schematic the LMV2011 is configured as a differential amplifier to feedback the actual voltage seen by the load minus any wiring voltage drops. The actual VOUT of the Voltage source is regulated to a value equal to the voltage required by the load plus the voltage drops in the wiring. In the above example, the LMV2011 with its near zero offset voltage and offset voltage drift, makes an excellent remote sensing amplifier.



Complete Sensor Bridge Interface

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The Art of Analog 30

Bridge based transducers are used in a variety of measurement instruments. The signal level from Bridges are typically low level ranging from several hundred microvolts to a few millivolts. The excitation voltage must be stable since changes in the excitation voltage can be interpreted as a bridge measurement signal. The circuit shown here address both of these issues.

The bridge excitation voltage uses a LM4140 voltage reference that has a 0.1% accuracy, and more importantly, a drift specification down to 3 PPM per degree C. This reference, in conjunction with the chopper stabilized buffer, A1, provides an ultra stable excitation voltage for the Bridge.

There are four key parameters for good performance of the bridge amplifier:

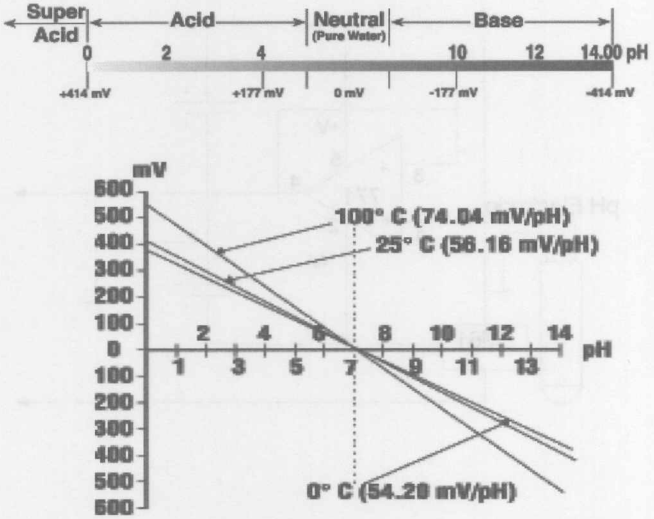
The output signal from the sensor bridge is combined with a common mode voltage. In many types of instruments the common mode voltage is about half the excitation voltage with the measurement signal as a small difference voltage between the legs of the bridge. These requires a high common mode rejection ratio (CMRR) to minimize the error introduced by the common mode voltage.

The input offset voltage and input offset voltage drift must be small compared to the differential signals from the bridge.

The input bias currents of the amplifiers must be small compared to the current flowing in each leg of the bridge.

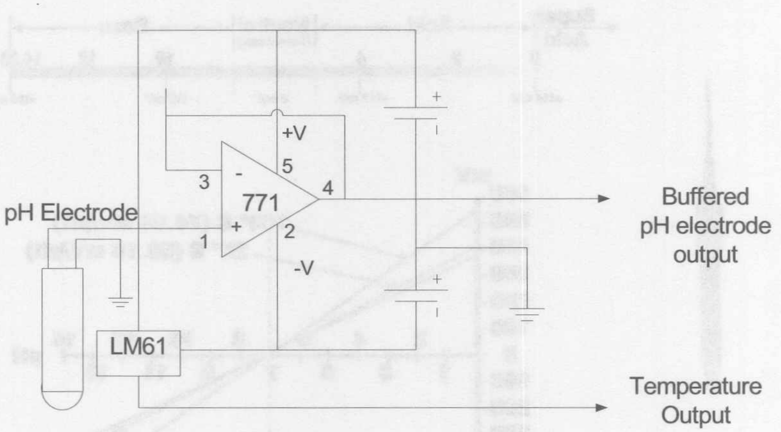
Amplifiers A2, A3, and A4 are used to construct an instrumentation amplifier to meet the requirements listed above. The total gain for this configuration is $A_V = (1 + 2R_2/bR_2)(aR_1/R_1)$

pH Electrode



The pH electrode is used to measure the pH of a solution. The graphs above show the physical relationship between the pH of a solution and the output voltage of the pH electrode and its temperature dependence. The source impedance of the pH electrode is typically 10^6 Ohms to 10^7 Ohms. For most practical uses the pH electrode must be buffered before driving the cable to the measurement instrument. Additionally, to obtain an accurate measurement of pH the temperature of the pH electrode must be known.

LMV771 pH Electrode Buffer



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The Art of Analog 32

In the application shown above the LMV771 is used to buffer the pH electrode while operating from two 1.5 volt batteries. The LMV771 has MOS input transistors with, typical input bias current of 0.1 pA and provides an excellent high input impedance for the pH electrode. The LMV771 has good output drive capability for transmitting the signal down the wire. The precision temperature sensor, LM61, will provide the temperature of the pH electrode. With this combination an accurate, temperature-compensated pH value can be measured.

LMH6624/26

- **Low offset voltage and wide bandwidth**
  - ***Ultrasound amplifiers***
  - ***Scintillation amplifier***
  - ***Medical imaging***

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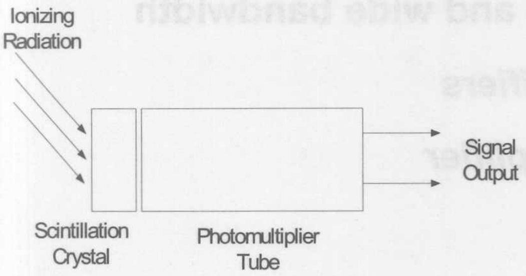
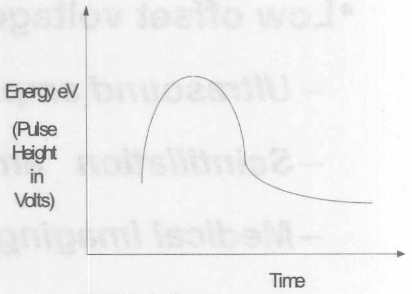
The Art of Analog 33

Several types of industrial and medical instrumentation require the accurate processing of high-speed signals prior to analog to digital conversion. The LMH6624 is a single amplifier and the LMH6626 is a dual amplifier. with good DC specs and a wide bandwidth.

Radiation Spectroscopy



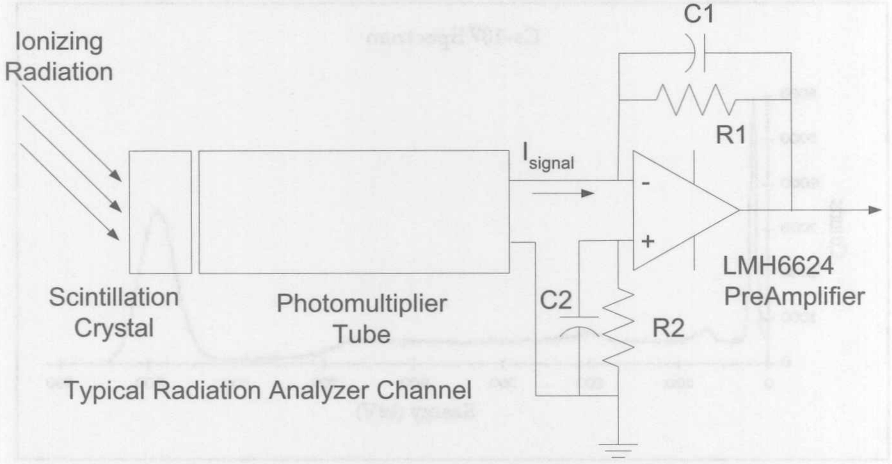
Typical Radiation Energy Measurement Instrument



Output pulse from
single photon

Radiation spectroscopy is the measurement of the distribution of energy emitted from a radiation source. The source radiation may be particles, x-rays or gamma rays. The radiation strikes the scintillation crystal and emits a short burst of light in which the intensity is proportional to the energy. The light is converted to a current and amplified by a photomultiplier tube.

Single Channel Analyzer



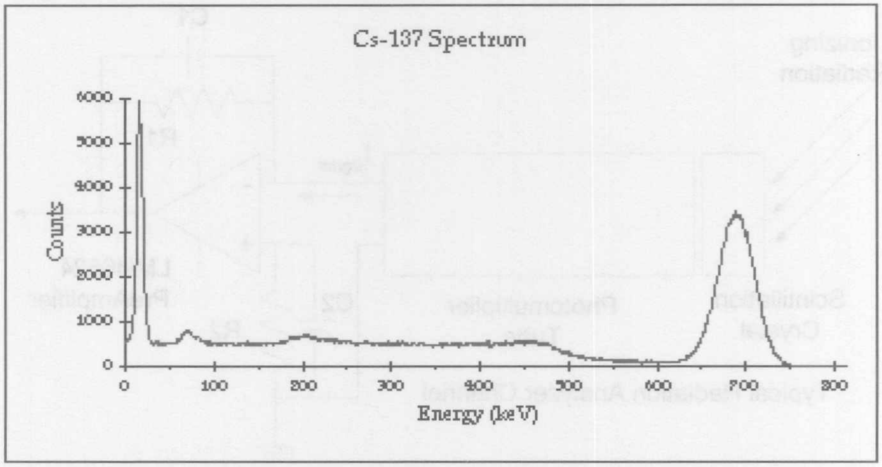
In the application above, the LMH6624 is is used as the preamplifier and current to voltage converter for the output of the photomultiplier tube. The circuit above represents a single channel analyzer used in basic radiation spectroscopy. The pulse amplitude of the signal contains the information of interest so a low input offset voltage and offset voltage drift is important. The wide bandwidth provides the fast response to process the pulse which can be which can be as short as several nanoseconds.

The feedback resistor in the schematic above can be calculated as follows:

$$R1 = (\text{Full Scale } e_{out})/(\text{Max } I_{signal}) \ ; \ R2 = R1$$

The output of the preamp makes its way to a pulse height analyzer, for example a fast A/D converter, to measure and bin the number of occurrences of each peak value. The distribution is the spectrum for that particular source.

Spectrum for Cs-137



The graph above represents the spectrum of a Cesium 137 source.

Precision Amplifiers

Precision amplifiers are required in a wide range of instrumentation to maintain fidelity to the original signal of interest

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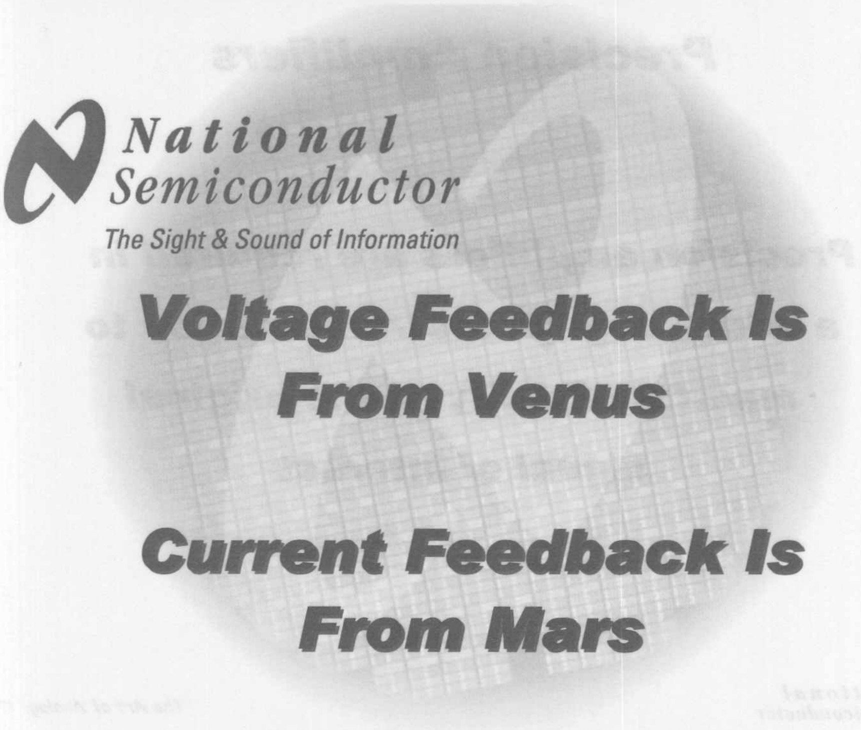
The Sight & Sound of Information

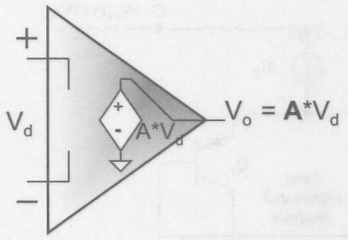


Voltage Feedback Is From Venus

Current Feedback Is From Mars

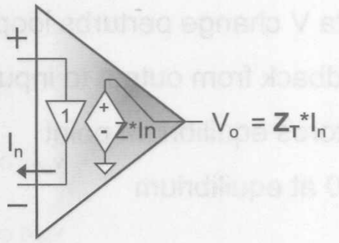
Op Amp Architectures

Voltage Feedback



- Both Inputs are High Impedance
- High Forward Voltage Gain A, (V_o/V_d)
- Low Output Impedance
- Error Signal is Vd
- Constant Gain x Bandwidth Product

Current Feedback



- Positive Input is High Impedance
- Negative Input is <u>Low</u> Impedance
- High Forward Transimpedance Gain Z_T, (V_o/I_n)
- Low Output Impedance
- Error Signal is In
- Bandwidth Independent of Gain (almost)

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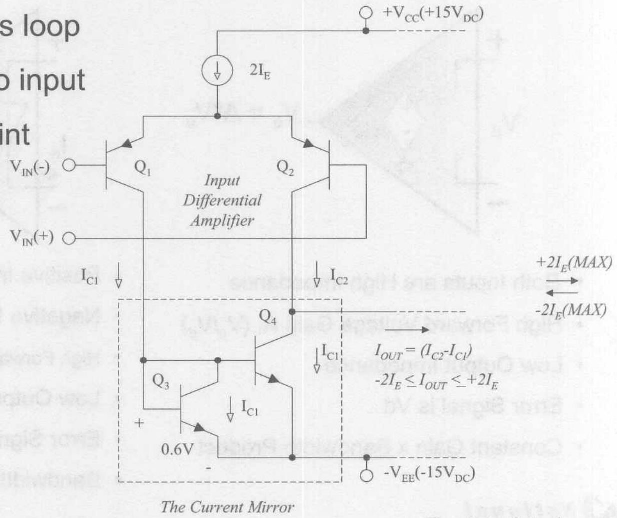
Here is a brief summary of the differences between voltage and current feedback op-amps. Voltage feedback op-amps employ a differential pair configuration such that the impedance at each input is high. The inputs of a current feedback (CFB) op amp are unbalanced as seen in the schematic on the right. The non-inverting input exhibits the high impedance normally associated with the voltage feedback (VFB) op amp. However, the inverting input of the CFB present a low impedance to the outside. This is because there is a unity gain buffer between the negative and positive inputs to the CFB. We shall see in the following foils that the error signal employed is also different. The error signal for the VFB is the delta voltage between the inverting and non-inverting inputs. The error signal for the CFB is the current IN flowing into or out of the non-inverting input. This characteristic accounts for the name, current feedback op-amp. A performance characteristic associated with this topology is the situation that the bandwidth of the amplifier is independent of the gain of the device. This contrasts with the VFB amplifier whose gain-bandwidth product is constant. This familiar curve slopes downward to the right for the VFB, as will be seen. Although the execution in internal circuitry is different, from the user viewpoint either may be used in the vast majority of applications.

VFB Amplifier – Feedback Activity

-Vin+ - Vin- controls loop

- delta V change perturbs loop
- feedback from output to input restores equilibrium point
- I = 0 at equilibrium

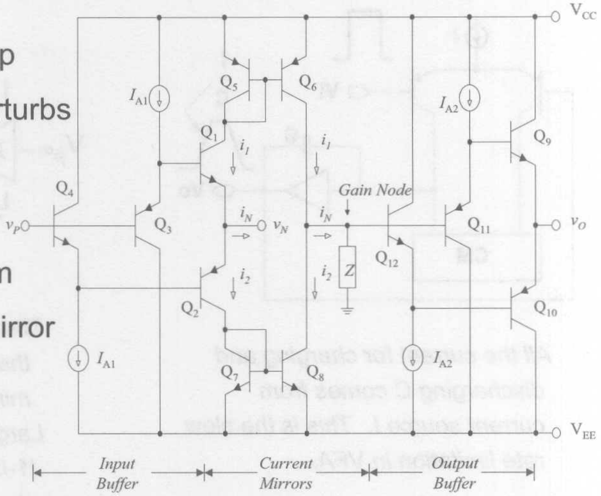


This foil reviews the feedback action of the VFB op-amp. Seen in the input stage circuitry are, from top to bottom, a current source of magnitude 2Ie, a differential pair Q1 and Q2, and a current mirror formed by Q3 and Q4 such the the current Ic1 is mirrored to Q4 causing both Ic1 current and Ic2 current to appear at the collector of Q4. The polarities are such that the delta current (Ic1-Ic2) appears as the input current to the next (2nd) stage of the amplifier. This is the classic VFB input stage topology.

Under the assumption of zero input voltage between Vin- and Vin+, Ic1 and Ic2 are equal and no delta current flows to the ouptut, hence no signal is transferred. A non-zero input signal on either input causes a delta current to flow to stage two. This signal is amplified in the interstage and the output stage of the amplifier. Feedback from the output to the inverting input closes the loop.

CFB Amplifier – Feedback Activity

- current at Vn controls loop
- current change at Vn perturbs equilibrium
- feedback current at Vn re-establishes equilibrium
- transistors Q6 and Q8 mirror currents in Q5 and Q7



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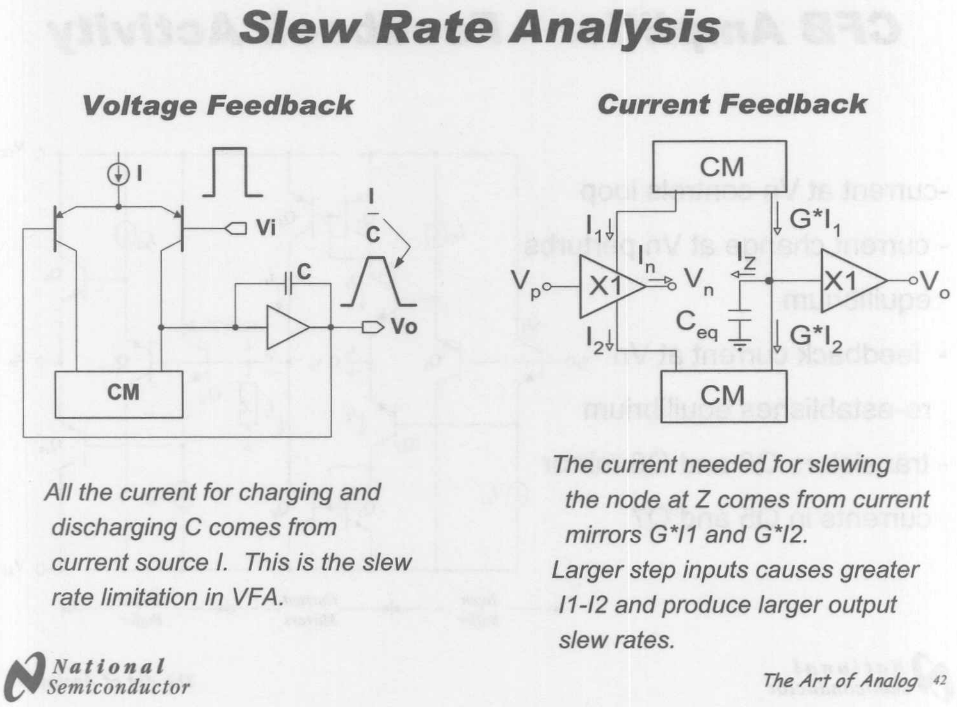
In a CFB op-amp, the rebalancing action caused by loop closure happens at the node Vn. Upon addition of feedback from the output to Vin-, current is added or subtracted from the In current, that is the current at the output of the input buffer between Vin+ and Vin-. In other words, the external network causes an inbalance between the currents of the push-pull pair, Q1 and Q2. The feedback current signal then functions to re-balance the current at Vn causing the system to faithfully reproduce at the output, the input signal with or without gain as the case may be. This current action in restoring equilibrium produced the designation current-feedback op-amp. To reiterate: in the voltage feedback op-amp, circuit equilibrium is restored based upon the difference voltage, Vin+ and Vin-. In the current feedback op-amp, circuit equilibrium is restored based upon the current condition at the Vin- node. Also note that the buffer currents i1 and i2, are mirrored at an increased amplitude by current mirrors Q5, Q6 and Q7, Q8. This will be important in the slew rate discussion that follows.



Slew Rate Analysis

Voltage Feedback

All the current for charging and discharging C comes from current source I. This is the slew rate limitation in VFA.

Current Feedback

*The current needed for slewing the node at Z comes from current mirrors G*I1 and G*I2.*

Larger step inputs causes greater I1-I2 and produce larger output slew rates.

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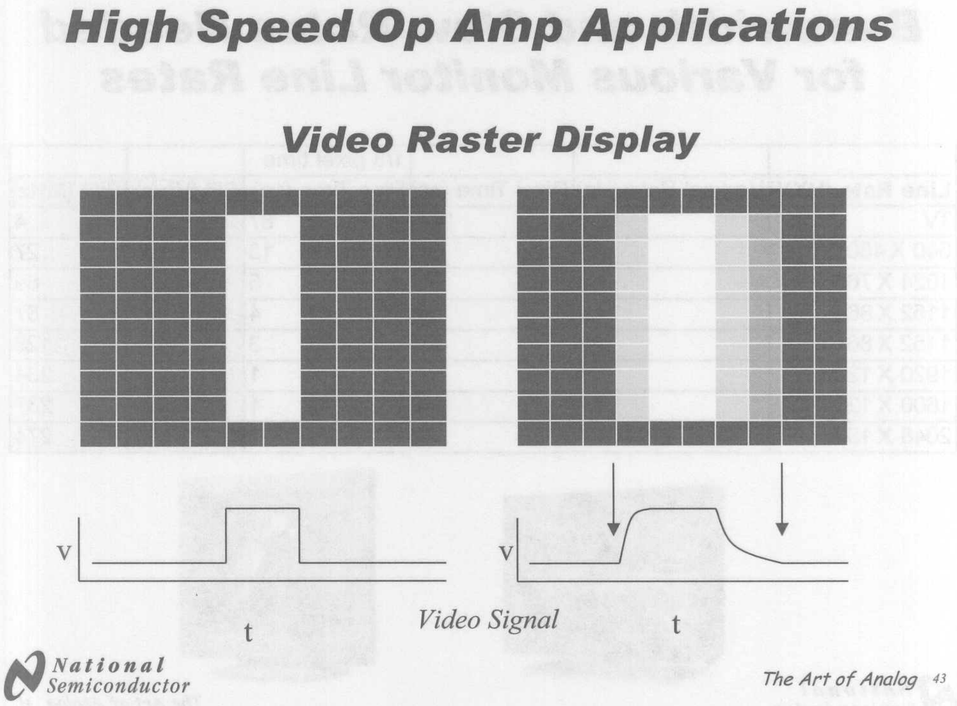
The Art of Analog 42

One of the two important differences between VFB's and CFB's is the capability of the CFB to produce higher slew rates than the VFB for the same quiescent current and process conditions. The other difference is the relative independence of gain and bandwidth in the CFB amplifier. The VFB op-amp is limited in slew rate by the ability of that circuit configuration to charge and discharge the interstage capacitor C in the voltage feedback schematic on the left. The current source I which supplies the balancing currents to the input differential pair, is the sole source of current available to charge and discharge C when the circuit is under large signal, slew rate conditions. Since a current source supplies the same current under all conditions, charging and discharging are limited to I, regardless of the magnitude of the input signal applied to the differential pair.
In the case of the CFB amplifier Ceq, the gain node capacitance is charged by the balanced current sources CM which produce current Iz. This becomes the charging and discharging current for Ceq. However, this current is not limited by the differential pair current source current as in the case of the VFB. Rather, Ceq is charged and discharged by the delta current Iz supplied by the current mirror. These matched current mirrors, CM, CM, are responding to the magnitude of In which is driven by the input signal. Thus, the charging current for Ceq, which becomes the slew rate limitation in a CFB op amp, is proportional to the input signal and would be theoretically limited only by the size of the current mirror transistors.



High Speed Op Amp Applications

Video Raster Display

Video Signal

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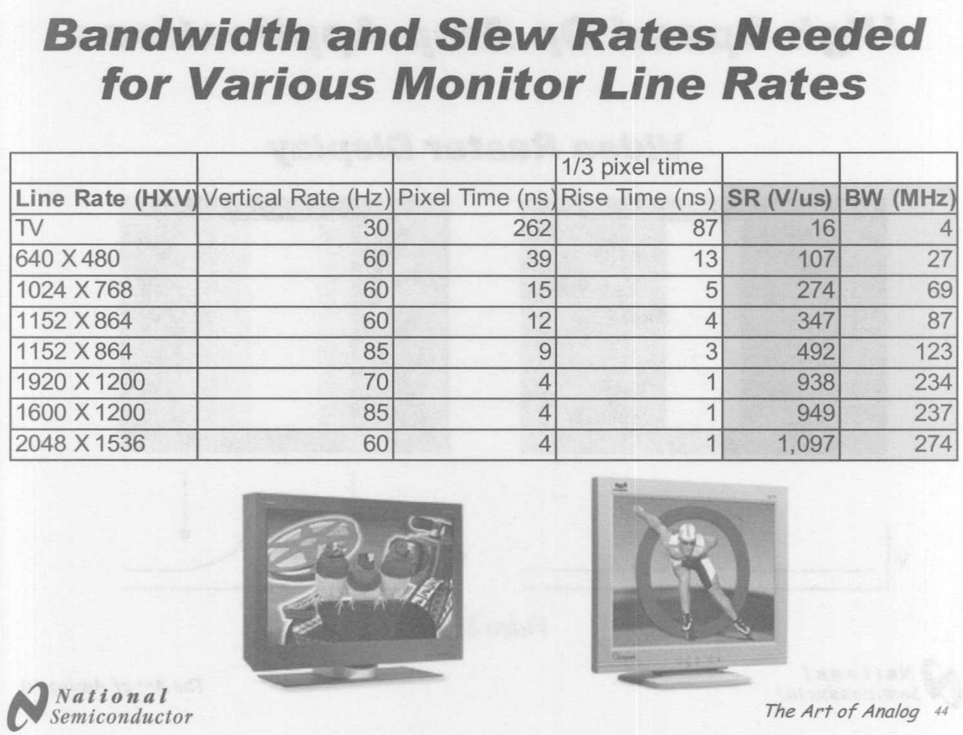
The Art of Analog 43

Rise and fall time are critically important to the faithful reproduction of video on a raster scan display. The black-to-white luminance signal amplitude of a video signal is such that video amplifiers should be chosen for both bandwidth and slew rate performance. Video signals for distribution are in the range of 1.5-2V. To faithfully reproduce video signals of high quality the overall speed and slew rate must be appropriate and the output drive capability must match the speed of the earlier stages. Understanding the slew rate performance is important because in most video designs, the intent is to avoid slew rate action in the amplifier as much as possible. A slew rate condition indicates the feedback control loop is unable to track the input signal for a portion of the input signal. Video circuits should be designed to avoid this condition. Higher bandwidth, lower settling time, and higher slew rate are all factors in keeping the feedback in operation throughout the input cycle. The clean black-to-white and white-to-black transitions shown on the left, require the clean drive signal shown below the drawings. Failure to faithfully reproduce the signal on the left due to amplifier limitations will result in the degraded signal shown in the lower right. This signal applied to a video display will produce the degraded result shown in the screen drawing on the upper right. A high-quality, high-speed amplifier with video speed, slew rate, and differential gain and phase specs is crucial to faithful video reproduction.



Bandwidth and Slew Rates Needed for Various Monitor Line Rates

			1/3 pixel time		
Line Rate (HXV)	Vertical Rate (Hz)	Pixel Time (ns)	Rise Time (ns)	**SR (V/us)**	**BW (MHz)**
TV	30	262	87	16	4
640 X 480	60	39	13	107	27
1024 X 768	60	15	5	274	69
1152 X 864	60	12	4	347	87
1152 X 864	85	9	3	492	123
1920 X 1200	70	4	1	938	234
1600 X 1200	85	4	1	949	237
2048 X 1536	60	4	1	1,097	274

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The Art of Analog 44

These are some of the more common line rates in use today. As it can be seen from this chart, at higher line rates, the BW and SR requirements on the op amp could be demanding. When used in a gain of +2 configuration amplifying and buffering a video signal, the amplifier output could see voltage excursions of up to 1.4Vpp. In every case shown here, it is assumed that the video could take as long as 1/3 the total pixel time in order to reach the final voltage (another 1/3 for keeping the pixel potential and the last 1/3 for reverting back). Obviously, in terms of SR, the worst case would be alternate white (on) and black (off) pixels.

Even though the video signal does not necessarily deal with sinusoidal waveforms, its speed can be effectively related to the sine wave concept of BW through the expression:

BW= 0.35/ [rise/fall_time]

This is the relationship between the rise time and the –3dB BW of a single pole roll-off gain curve. Even though most systems are not exactly "single-pole", this relationship is a good approximation. The terms rise time is generally reserved for "small signal" and it refers to the time it takes the signal to travel between 10% and 90% of the final voltages. Generally speaking, an amplifier rise time would start to deteriorate as the amplitude is increased if the Slew Rate required is larger than what the amplifier is capable of. In a voltage feedback amplifier, this is generally set by the amount of current available to charge the internal dominant pole capacitor.

For the SR, the corresponding analogue between the time and frequency domain is:

$SR=2*\pi*Vp*f$

where: π=3.14, Vp= Peak voltage of the highest sinusoidal frequency, f=highest frequency

So, a 10MHz, 2Vpp sine wave would need an amplifier which has a SR larger than 63V/us in order to not be slew rate limited.

In the chart shown here, the SR number is approximated by dividing the total change in voltage by the 10-90% rise time. This is a good conservative approximation especially because the SR specification for an op amp is sometimes nebulous in its definition.

Some High-Speed Op Amps For Video Applications

National CFB Video Amps			
	Slew Rate V/µS	BW	DG/DP
LMH6714/20/22	1800	400	.01/.01
LMH6718	600	110	.04/.03
LMH6715	1300	400	.02/.02
LMH6732*	2700	540	.025/.01
LMH6702	3100	720	.025/.004
LMH6181	1400	100	.05.04
LMH6559	4580	1750	.06/.02
LMH6560	2700	680	.1/.03

**programmable*

National VFB Video Amps			
	Slew Rate V/µS	BW	DG/DP
LMH6642/3/4	125	135	.01/.01
LMH6654/5	200	130	.01/.025
LMH6657/8	700	100	.03/.01
LMH6639	170	145	.012/.045
LMH6628/3	940	180	.01/.08
LMH6502/3	1800	130	.34/.10
LMH6609	1400	280	.01/.025

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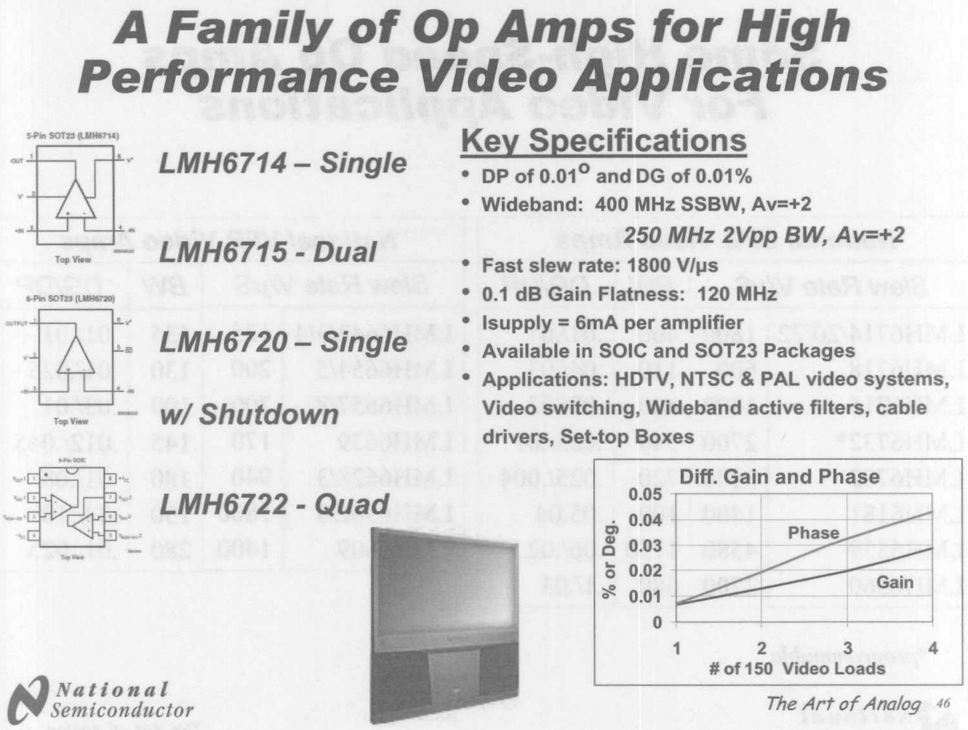
National Semiconductor designs and manufactures a family of high performance video integrated circuits. Both VFB and CFB topologies along with a wide selection of speeds, packages and features. Each of these video devices is characterized for differential gain and differential phase as seen in the above table. National's advanced VIP10 process with trench isolation and bonded wafers are capable of the type of advanced specifications needed for high performance video processing.



A Family of Op Amps for High Performance Video Applications

LMH6714 – Single

LMH6715 - Dual

LMH6720 – Single w/ Shutdown

LMH6722 - Quad

Key Specifications

- DP of 0.01° and DG of 0.01%
- Wideband: 400 MHz SSBW, Av=+2
  250 MHz 2Vpp BW, Av=+2
- Fast slew rate: 1800 V/µs
- 0.1 dB Gain Flatness: 120 MHz
- Isupply = 6mA per amplifier
- Available in SOIC and SOT23 Packages
- Applications: HDTV, NTSC & PAL video systems, Video switching, Wideband active filters, cable drivers, Set-top Boxes

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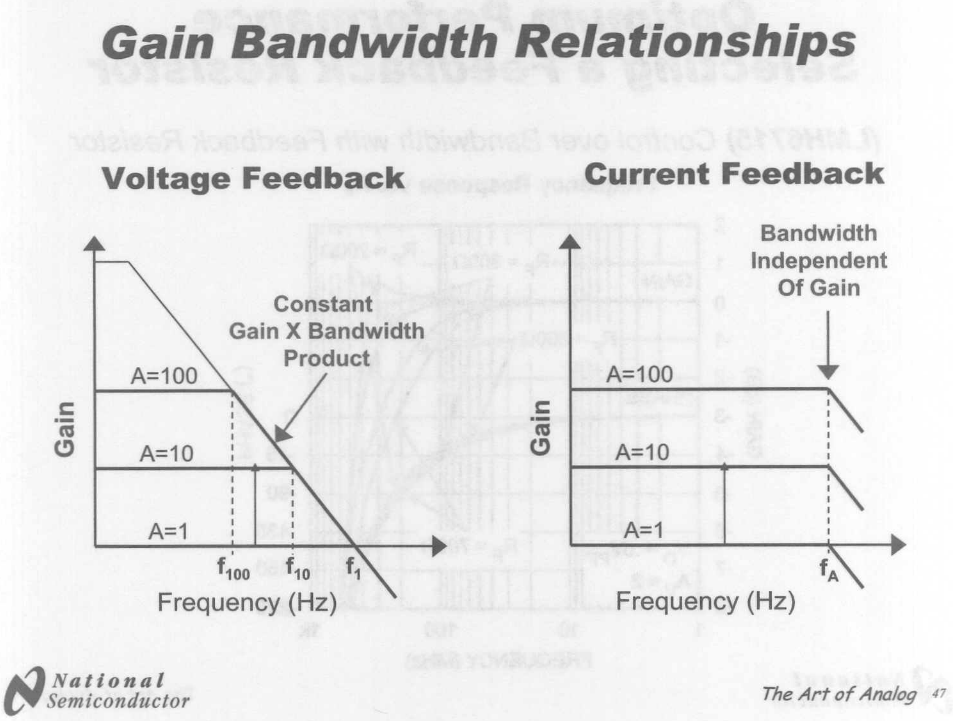
The Art of Analog 46

National Semiconductor makes high-performance video ICs in a variety of configurations and packages. The LMH6714/15/20/22 family features excellent differential phase and gain specifications of 0.01 degrees and 0.01% respectively. These devices exhibit gain flatness of 0.1 dB out to 120 MHz. The single, dual and quad versions are the LMH6714/15/and LMH6722 respectively. The single with shutdown is designated the LMH6720. These current feedback devices provide a 2Vpp bandwidth of 250MHz typical, and a slew rate of 1800V/us. These ICs are well suited for middle and high end video applications in video switching, cable systems, and set-top boxes.



Gain Bandwidth Relationships

Voltage Feedback **Current Feedback**

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The Art of Analog 47

Another important difference between the VFB op-amp and the CFB op-amp is in the inherent relationship between gain and bandwidth. The VFB produces a constant gain times bandwidth product as diagrammed in the left hand figure above. If the external circuit is configured for a gain of 100, the maximum frequency for which the circuit will faithfully reproduce a sine wave input at the output is 1/100 of the frequency that such an input signal will be faithfully reproduced if the external configuration is for a gain of 1. This relationship is easily remembered as the gain-bandwidth product for the IC. The point of inflection for an op-amp is very low, of the order of a few hertz for low frequency VFB op-amps and in the range of 5 to 10KHz for high speed VFB amplifiers. The slope of the gain-bandwidth product is the familiar one pole roll-off, of 6db per octave or 20db per decade.

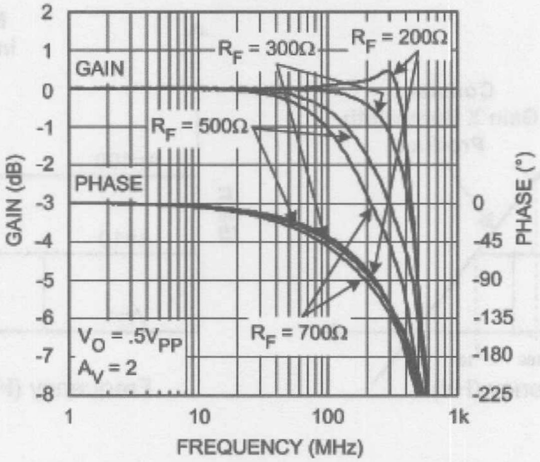
In the case of the CFB op-amp, the gain setting based upon the external components is independent of the frequency over the meaningful range of operation of the CFB. Beyond the commencement of roll-off at point f_A the CFB amplifier exhibits the frequency attenuation characteristics of the VFB. This relationship allows for increased performance in terms of distortion and bandwidth per milliamp of supply current at high frequencies. The CFB amplifier is less flexible in terms of external components than is the VFB amplifier. This will be seen in the limitations on the selection of the feedback resistor, R_F as will be discussed in the next foils.

An important advantage in the area of distortion can be seen from these diagrams. Take an example of a circuit operating at a gain of ten and an operating frequency indicated by the vertical arrows in the diagrams. In the case of VFB, the higher harmonics of the operating frequency will be attenuated due to the slope of the gain-bandwidth product curve. In the CFB case on the right, more of the higher harmonics are reproduced and the resultant is lower harmonic distortion, particularly of the higher harmonics of the fundamental.

Optimum Performance Selecting a Feedback Resistor

(LMH6715) Control over Bandwidth with Feedback Resistor

Frequency Response vs. R_F



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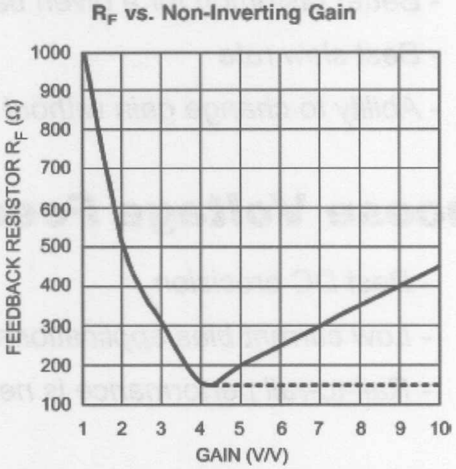
The Art of Analog 48

Unlike the VFB op-amp which allows a very wide range of feedback resistor values, the range of values for the feedback resistor, Rf in a CFB op-amp are specified as a design parameter. Within the allowable range, however the equipment design engineer can control the response of the amplifier particularly with regard to the amount of peaking needed in the circuit design. This chart show empirical data for one National Semiconductor current feedback op-amp, the LMH6715. The gain is fixed at +2 and the amplitude and phase is plotted for a range of frequencies. Higher values of Rf such as 700 ohms results in the onset of amplitude roll-off at a lower frequency than does a lower value Rf such as 300 ohms. For example, a 700 ohm Rf produces a 1dB roll-off at 100 MHz, whereas a 300 ohm resistor produces a 1dB roll-off at 300 MHz. Notice the the phase response for each does not change dramatically. Also, note that the Rf range is confined to the range of 200 ohms to 700 ohms.

Selecting a Feedback Resistor For CFA

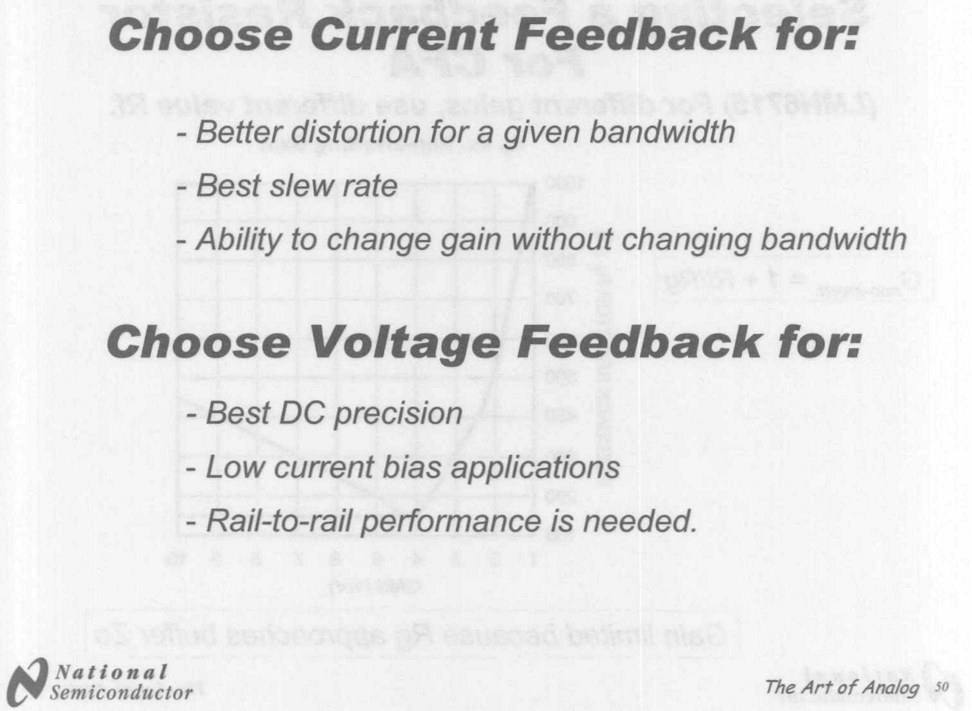
(LMH6715) For different gains, use different value Rf.

$G_{non\text{-}invert.} = 1 + Rf/Rg$



Gain limited because Rg approaches buffer Zo

Another decision in the design of CFB amplifier circuits is that of gain to be taken. In this case we are referring to non-inverting gain which is the normal situation for CFB design. The chart graphs recommended gain settings against choices for feedback resistor Rf. Here as in the prior example, the range of values is confined to a specific range, from around 200 to 800 ohms. As the Rf value is reduced the amount of gain that is allowed becomes limited because the value of the Rg resistor in the gain equation for the non-inverting op-amp begins to approach the value of the input buffer output impedance, seen at the negative input. In other words if an Rf value of 200 is chosen, a gain choice of 4 would result in an Rg resistor value of 50 ohms. The output impedance of the input buffer is around 180 ohms; therefore 50 ohms would be a practical lower limit for Rg. Because of this phenomenon, designs requiring gains greater than 5 are indicated to have increasing values of feedback resistors as seen by the ascending curve in the diagram.



Choose Current Feedback for:

- Better distortion for a given bandwidth
- Best slew rate
- Ability to change gain without changing bandwidth

Choose Voltage Feedback for:

- Best DC precision
- Low current bias applications
- Rail-to-rail performance is needed.

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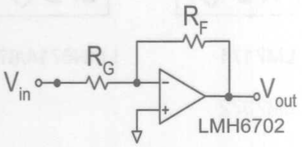
The Art of Analog 50

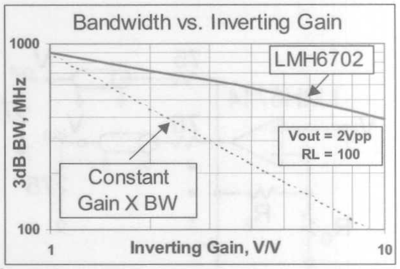
Voltage feedback op-amps and current feedback op-amps each have their own range of recommended applications. CFB amplifiers are indicated when slew rate and exceptional low distortion are needed. VFB amplifiers excel for DC applications, for applications requiring low input bias current (or high input impedance), and where rail-to-rail performance is critical. As a general rule CFB amplifiers will be offered for high speed applications, whereas VFB amplifiers are ubiquitous and used for low, medium, and high speed applications.

LMH6702 – Ultra-Low Distortion Amplifiers

Key Features *(Typical Values, unless noted)*

- Ultra low distortion: Vout = 2Vpp, RL = 100
  - -90 dBc HD3 @ 10MHz
  - -70 dBc HD3 @ 60MHz
- Wideband: 2GHz SSBW, Av=+1
- Very high slew rate: 3100 V/us
- Low voltage noise: 1.8 nV/sqrt (Hz)
- Isupply = 12.5 mA
- Packages: SOIC-8 and SOT23-5
- Applications: A/D driver, D/A trans-impedance buffer, wide dynamic range IF amp, radar/comm. receivers, high resolution video

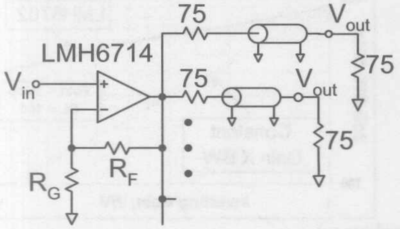




For applications that need a combination of very high speed and very low distortion National's new LMH6702 current feedback op-amp is compelling choice. Exceptional distortion specifications are required for applications such as driving fast A/D converters, in wide dynamic range IF amps such as in base stations, for high resolution video, and for applications where multiple RF carriers are present. Third harmonic distortion of 90dBc and 70dBc at 10MHz and 60MHz respectively represent excellent distortion performance in an integrated circuit.

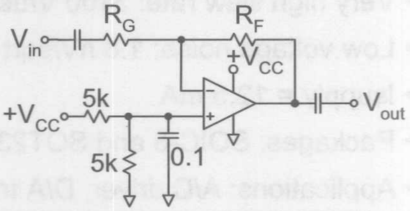
Distribution Amp

VFB ✓	CFB ✓
LM7171 LM7372	LMH6714/6720/6722



AC Coupled Single-Supply Amplifier

VFB ✓	CFB ✓
LMH6642/43/44 LM7171 LM7372 LMH6654/6655 LMH6682/6683 LMH6657/6658	LMH6714/6720/6722 LMH6732 (adj. BW) LMH6702L



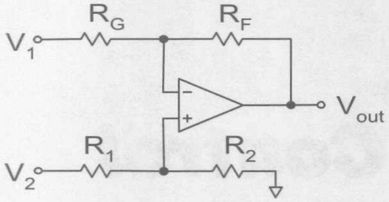
Favor VFB when input signal needs to swing to either supply rail.

Favor CFB for high quality, high resolution video distribution.

Certain high speed applications may be achieved with either a voltage feedback or a current feedback amplifier approach. Show in the drawing on the left is a video distribution amplifier. National amplifier IC that would be appropriate choices are listed above the diagram. On the right is an AC coupled single-supply amplifier and possible amplifier choices for this design. The LMH designator for National Semiconductor amplifiers indicates that the ICs are fabricated on National's new high speed VIP10 process.

Diff Amp

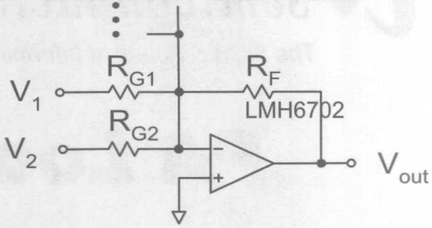
VFB ✓ **CFB ✓**



$$V_{out} = V2\left(\frac{R2}{R1+R2}\right)\left(1+\frac{RF}{RG}\right)\ V1\left(\frac{RF}{RG}\right)$$

Summing Amp

VFB ✓ **CFB ✓**



$$V_{out} = \ RF\left(\frac{V1}{RG1}+\frac{V2}{RG2}+\right)$$

Favor VFB for precision applications requiring high CMRR or when low noise in the presence of high source impedance is required.

Favor CFB when signals with disparate gain requirements must be summed at equal bandwidth.

Both VFB and CFB amplifiers may be configured as either a summing amp or a difference amplifiers. Feedback in each case appears at the minus input. In the case of the summing amplifier application, the negative input is the summing junction. Note that in the equation for the difference amplifier configuration, the first resistor term represents an attenuation factor for the applied signal, V2. While the CFB does have limitations in implementation, this foil illustrates that the CFB op-amp is still very versatile.

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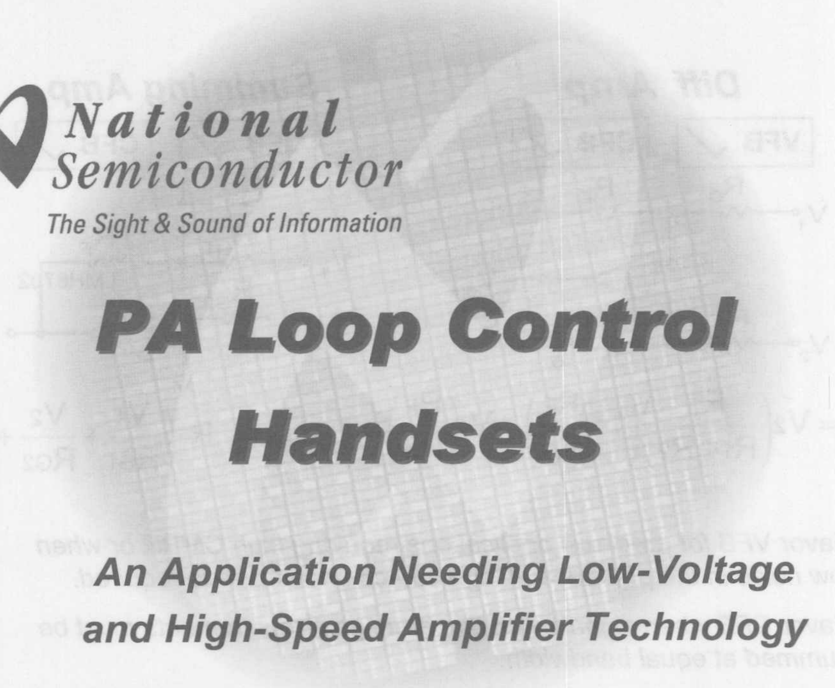
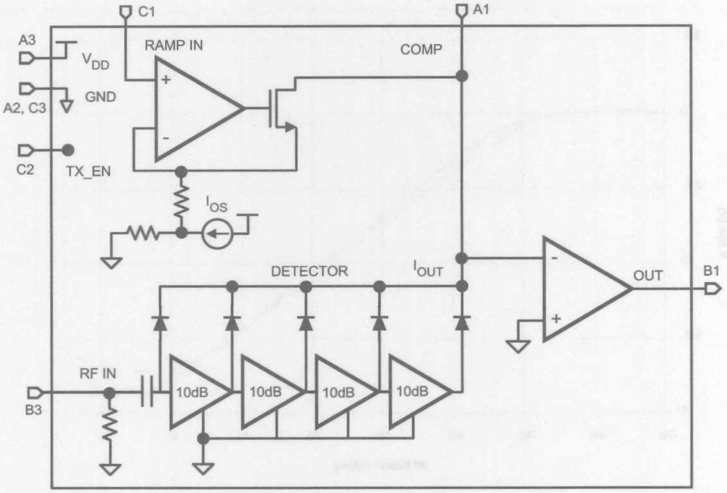
The Sight & Sound of Information



PA Loop Control Handsets

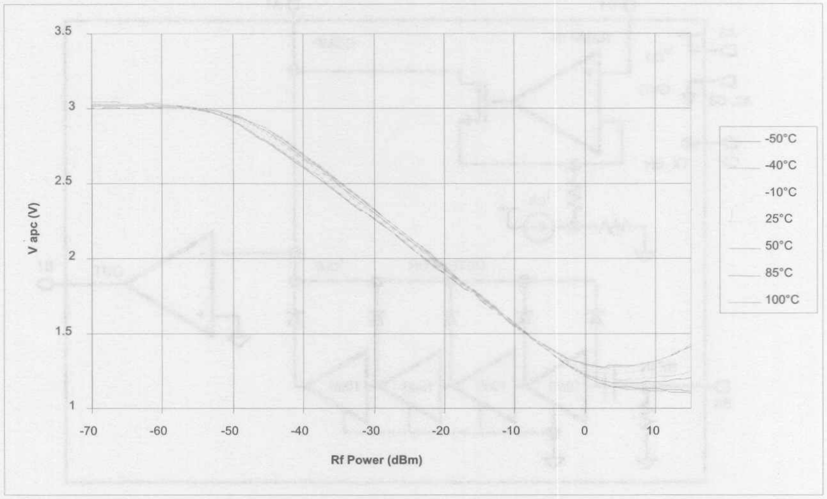
An Application Needing Low-Voltage and High-Speed Amplifier Technology

LMV243 Block Diagram

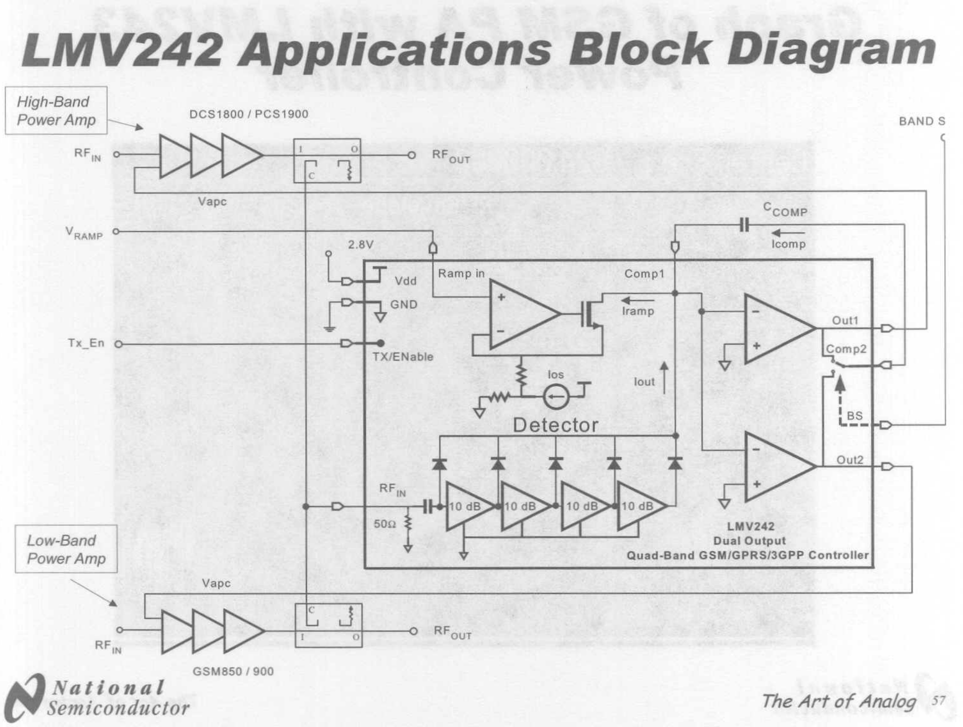


The LMV243 is a second-generation power amplifier controller for GSM/TDMA cellular handsets. The application requires the control IC to accept a ramp input from a baseband chipset, to detect transmit power received from an external directional coupler, to close a feedback loop with an error amplifier, and to deliver an output voltage which controls the handset PA. In the LMV243 internal circuit block diagram, the RF IN pin is internally terminated by a 50Ω resistor to ground and a capacitor which serves to block DC. The four stage log amplifier is composed of 4 10db gain stages alternating with five stages of RF detection. The result is a 40db detection range that is linear-in-dB. This log-amplifier detector determines the linear-in-dB characteristics of LMV243. The internal op-amp (C1 input) serves as a voltage-to-current converter. The error amplifier op-amp is seen on the right side and feeds the output pin, B1. This error amplifier is used to close the control loop in GSM Power Amplifier Control.

LMV243 Detector Performance Over Temperature – 900MHz



The characteristic curve of the log-amp detector in LMV243 is shown above. The overall linearity, the 40db range, and the minimum variation with temperature is evident in the RF power versus voltage plot of the LMV243.



LMV242 Applications Block Diagram

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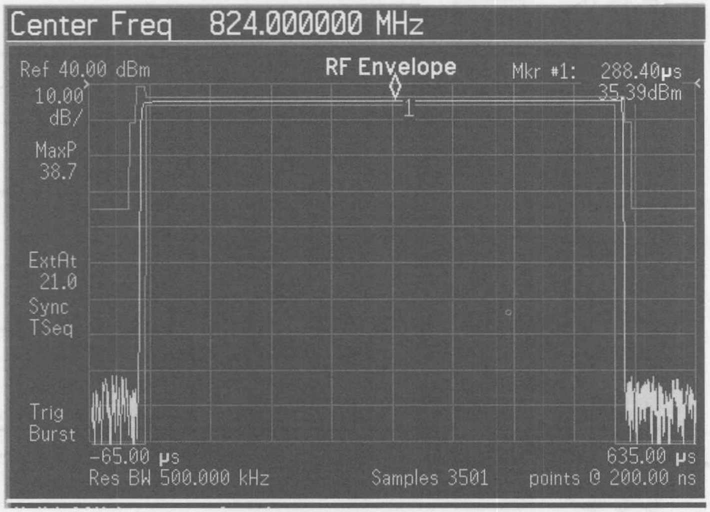
The LMV242 is a third-generation PA loop controller. In a quad-band GSM handset there is a high-band RF power amplifier for the DCS1800 and PCS1900 and another low-band RF power amplifier for GSM850 and GSM800 bands. The RF signal will be fed into the input of each PA one at a time and the corresponding Vapc pin is activated by the LMV242 controller. Assume that the low-band power amplifier is on and the high-band power amplifier is off. The GSM signal is fed into the input of LMV242 through a directional coupler. The log-amp detector of LMV242 will rectify the RF signal into dc current. The output current of the detector Iout drives the inverting input of an op-amp, configured as an integrator. A reference voltage drives the non-inverting input of the op-amp. This will be the ramp signal that defines the power profile for GSM to be transmitted. Finally, the output of the op-amp integrator drives the gain control pin (Vapc) of the power amplifier.

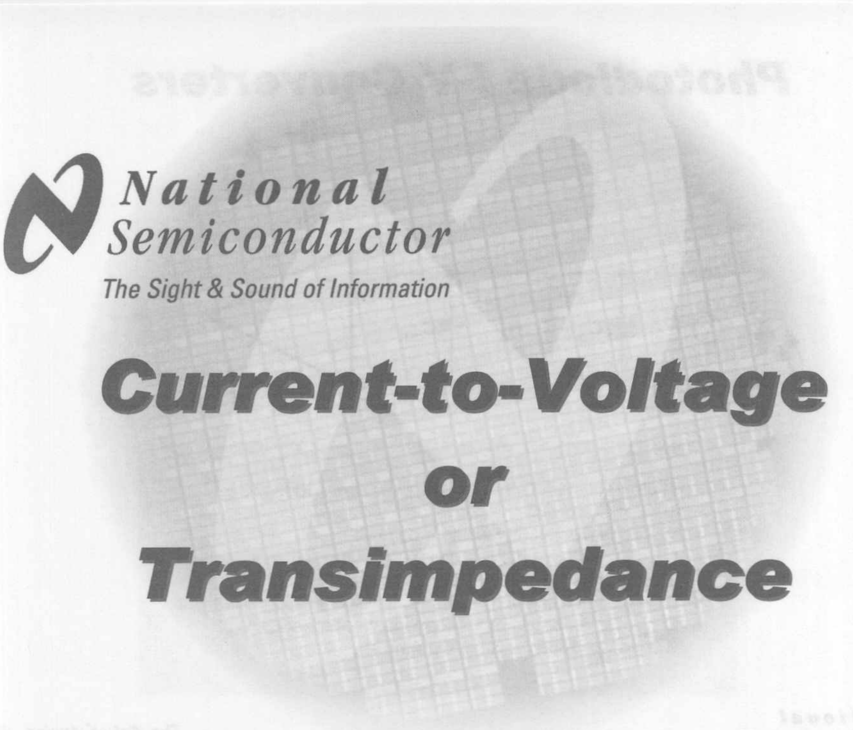
Now to examine how this circuit works, we will assume initially that the output of the PA is at some low level and that the Vramp voltage is at 1V. The V/I converter converts the Vramp voltage to a sinking current Iramp. This current can only come from the integrator capacitor Ccomp. Current flow in this direction increases the output voltage of the integrator. This voltage, which drives the PA, increases the gain. The gain will increase, thereby increasing the amplifier's output level until the detector output current equals the ramp current Iramp. At zero the integrator output will be held steady, thereby settling the loop. If capacitor charge is lost over time, the gain will decrease. However, this leakage will quickly be corrected by additional integrator current from the newly reduced detector current.

The LMV242 is intended for module PAM applications and is available in die form.

Graph of GSM PA with LMV243 Power Controller



In GSM transmitter testing, the power amplifier is required to pass the time-mask standard profile. The graph was a test result of a GSM power amplifier with LMV243 as a Power Amplifier Controller (PAC). Notice that in all cases, the detected power output falls within the GSM standard mask for cellular transmissions.



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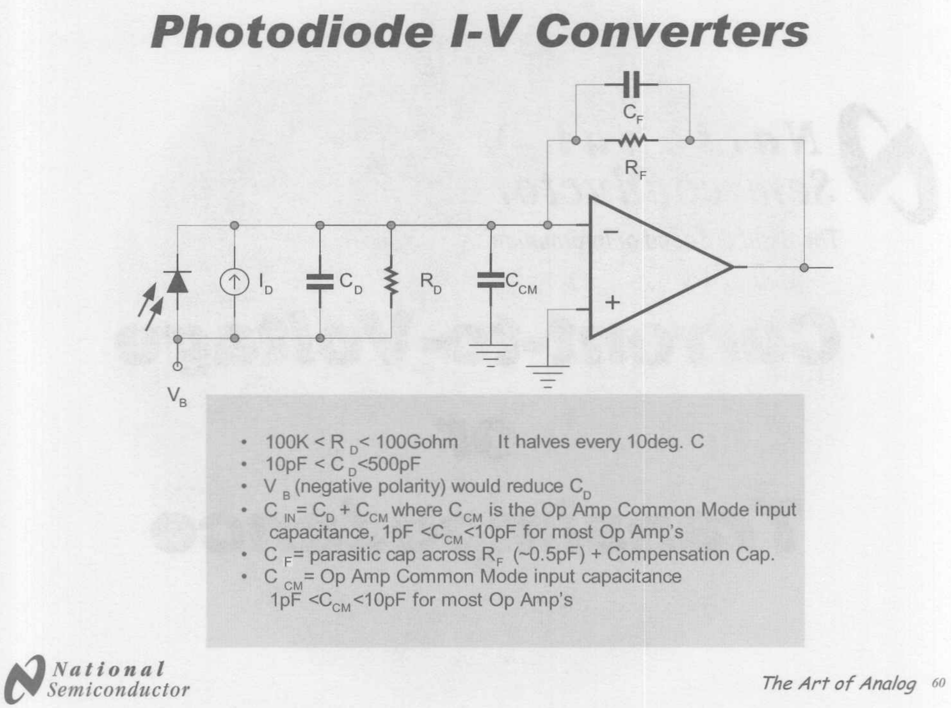
Current-to-Voltage or Transimpedance



Photodiode I-V Converters

- 100K < R_D < 100Gohm It halves every 10deg. C
- 10pF < C_D <500pF
- V_B (negative polarity) would reduce C_D
- $C_{IN} = C_D + C_{CM}$ where C_{CM} is the Op Amp Common Mode input capacitance, 1pF < C_{CM} <10pF for most Op Amp's
- C_F = parasitic cap across R_F (~0.5pF) + Compensation Cap.
- C_{CM} = Op Amp Common Mode input capacitance 1pF < C_{CM} <10pF for most Op Amp's

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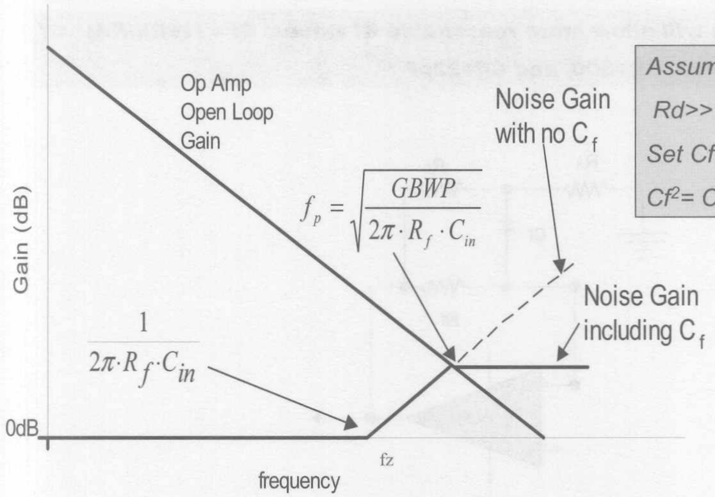
The Art of Analog 60

There are many applications which use photo diode to detect the intensity of the incident light. Examples would be: Barcode scanners, light meters, fiber optic receivers, industrial sensors, etc. The diode has a nearly linear output current for a very large range of light intensity. The voltage across the diode is held constant in order to minimize non-linearities.

Here is a schematic of a typical circuit used to convert the diode current into a voltage, along with the parasitic components of the diode and the amplifier. The op amp is an ideal candidate to do this since it has minimal input current and its high open loop gain will eliminate voltage variations at the Cathode. The higher speed applications could tie the Anode side to a negative potential in order to reduce the diode capacitance. As we shall see later, this capacitance is troublesome in two ways: It reduces the achievable bandwidth and necessitates stability compensation. Also, it tends to increase noise gain, as will be shown later. More sensitive diodes will tend to be of bigger area and will subsequently exhibit a higher capacitance. Rf determines the overall circuit sensitivity. So, one obvious tradeoff would be between raising the value of Rf (with resulting higher noise and lower BW) vs. increasing the diode area and having a larger Cd. In this schematic, Cin, the op amp's input capacitance is also included since it cannot be ignored in most cases.

Bode Plot Illustrating C_F Selection



Assume:

Rd>> Rf & Cin>> Cf, then:

Set Cf to cancel fp:

*Cf^2= Cin/(GBWP*2pi*Rf)*

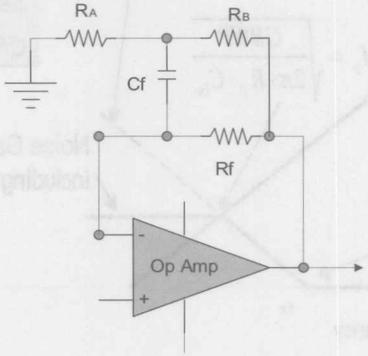
One interesting aspect of this type of amplifiers, also know as I-V converters, is that in almost all cases the frequency response needs to "shaped" or otherwise the circuit will oscillate. The high capacitance of the diode (including the op amp input capacitance), along with large Rf needed to get reasonable trans-impedance gain, will create enough phase shift around the loop that necessitates steps be taken to avoid oscillations.

As can be seen here, if Cf were not included, the noise gain plot would intersect the op amp open loop gain plot at a rate of closure of 40dB/decade. The noise gain is inverse of the feedback factor function. A zero in the noise gain corresponds to a pole in the feedback factor. Therefore, with no Cf, at the intersection point there is 180 degrees of phase shift and thereby oscillation would set in.

In order to operate properly, Cf would need to be chosen properly to set the noise gain pole to coincide with the op amp open loop gain plot as shown. This leads to a closed loop phase margin of 45 degrees. Under these conditions, the noise gain pole would be at the frequency shown (fp). This would be the BW of the I-V converter as well. If Cf is any larger, then the BW is excessively reduced.

Realistic Values

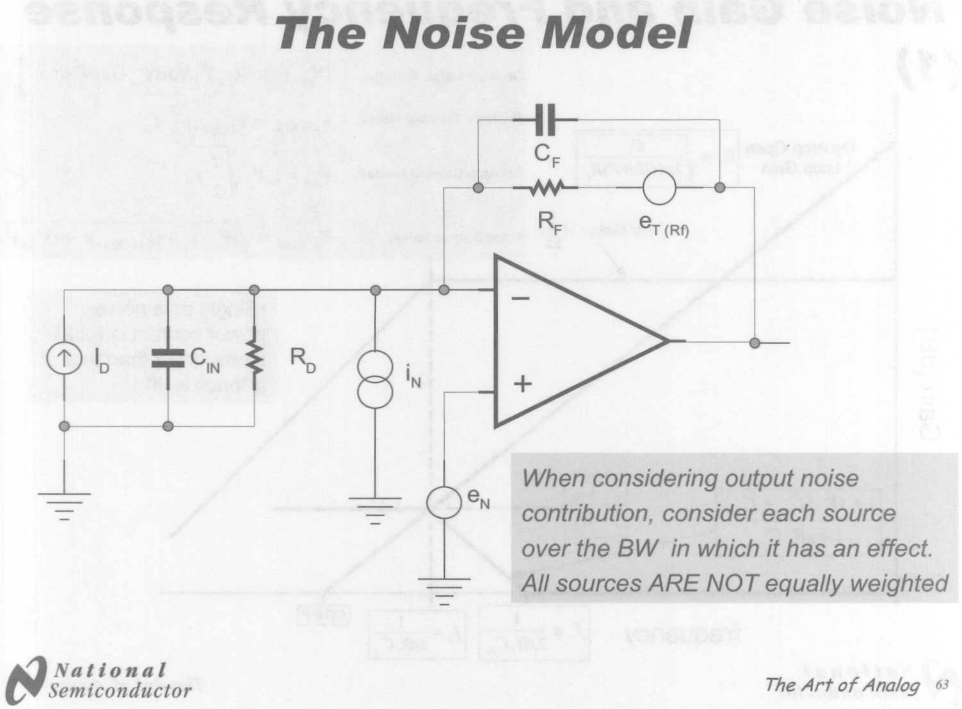
- **Network shown will allow more reasonable Cf values: Cf'= (1+RB/RA)* Cf**
- **For Cf=2pF, RA=50, RB=500, and Cf'=22pF**



Often, the required Cf would be very small (<5pF), especially for the higher speed applications. In these cases, its often more practical to use the circuit above in order to allow more reasonable values.
The new value of Cf'= (1+RB/RA)* Cf
This relationship holds true as long as RA<<Rf.

As an example, if Cf=2pF, , select RA=50ohm,and RB=500ohm.
Therefore, Cf'=(1+500/50)*2pF= ~22pF
which is a much more practical component value.

This value needs to be "fine tuned" in the real application for proper step response.



The Noise Model

When considering output noise contribution, consider each source over the BW in which it has an effect. All sources ARE NOT equally weighted

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The Art of Analog 63

Here is the noise model for the I-V converter. When doing noise analysis, as always, all noise sources can be assumed to be independent of each other thereby allowing the response to be calculated by considering one noise source at the time. The final output noise would be the RMS (root mean square) of the individual noise sources contributions to the output voltage.

Input capacitances have been combined into a single Cin. The noise current on the non-inverting input has been ignored since it won't contribute to any noise at the output.

The thermal noise voltage of any resistor is 4nV* √[R(Kohm)]. Therefore, a 100Kohm resistor would have 40nV/√Hz of noise at 25°C. This noise would increase at the rate of √[Temp(K)]. So, going from 300°K to 400°K increases the noise by a factor of 1.15.

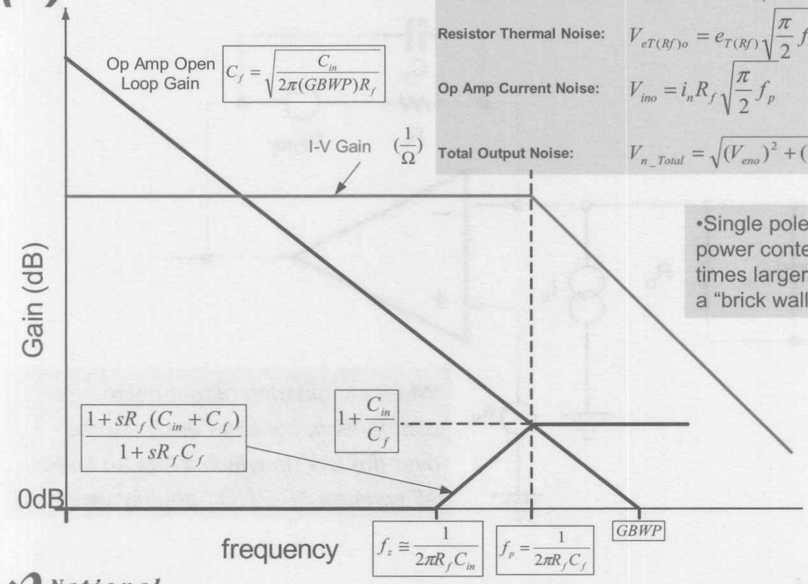
Noise Gain and Frequency Response (1)

Op Amp Noise Voltage: $(V_{eno})^2 \cong (e_n)^2 |Noise\_Gain|^2 df \times \frac{\pi}{2}$

Resistor Thermal Noise: $V_{eT(Rf)o} = e_{T(Rf)}\sqrt{\frac{\pi}{2} f_p}$

Op Amp Current Noise: $V_{ino} = i_n R_f \sqrt{\frac{\pi}{2} f_p}$

Total Output Noise: $V_{n\_Total} = \sqrt{(V_{eno})^2 + (V_{eT(Rf)0})^2 + (V_{Ino})^2}$



- Single pole noise power content is (pi/2) times larger than that of a “brick wall”

When analyzing the noise at the output of the I-V converter, its important to note that the various noise sources (i.e. op amp noise voltage, feedback resistor thermal noise, input noise current, etc.) do not all operate the same frequency band. Therefore, when the noise at the output is calculated, this should be taken into account. Namely, the op amp noise voltage will be gained up in the region between the noise gain’s “zero” and its “pole”. The higher the value of Rf and Cin, the sooner the noise gain peaking starts and the larger would be it’s contribution to the total output noise. Therefore, its obvious to note that its advantageous to minimize Cin (e.g. by proper choice of op amp, by applying a reverse bias across the diode at the expense of excess dark current and noise). Unfortunately, most low noise op amps have a higher input capacitance compared to ordinary ones.
The “π/2” factor within the square root will account for the single pole response.

For the op amp noise voltage, the calculation is slightly more complicated since the total noise contribution would involve an integration as the noise gain varies with frequency.

To maximize the I-V bandwidth for a given trans-impedance gain and photodiode, one would choose an Op Amp with high GBWP and low input capacitance. However, the input capacitance for an Op Amp is not always readily available on the data sheet.

Noise Gain and Frequency Response (2) An Example

$e_n = 10nV/\sqrt{Hz}$ $i_n = 3pA/\sqrt{Hz}$

$f_z = 100KHz$ $f_p = 1MHz$

C_{in}=50pF, C_F=5pF, R_F=32K

- The low frequency portion of the voltage noise contribution is negligible
- Between f_z and f_p, the Noise Gain is approximated by a +20dB/decade response having a "zero" at f_z: [Noise Gain (f)]^2=1+f^2/f_z^2

$$(V_{eno}')^2 = [10(\frac{nV}{\sqrt{Hz}})]^2.\{\int_{f_z}^{f_p}(1+\frac{f^2}{f_z^2})df + 100(KHz)\}$$

$$= 100e-18.\{\int_{100KHz}^{1MHz}(1+\frac{f^2}{(100KHz)^2})df + 100e3\}$$

$$= 100e-18.\{[f + \frac{f^3}{3\times(10e9)}]_{100KHz}^{1MHz} + 100e3\}$$

$$= 100e-18\times\{34.2e6 + \cancel{100e3}\} \cong 100e-18\times 34.2e6 = 3.43e-9(V^2)$$

$$V_{eno} = V_{eno}'\times\sqrt{\frac{\pi}{2}} = 73.4(\mu V)$$

$$V_{eT(RF)} = e_{T(Rf)}\times\sqrt{\frac{\pi}{2}\times f_p} = 4(\frac{nV}{\sqrt{Hz}})\times\sqrt{32}\sqrt{\frac{\pi}{2}\times 1e6} = 28.4(\mu V)$$

$$V_{ino} = i_n\times R_f\times\sqrt{\frac{\pi}{2}\times f_p} = 3(\frac{pA}{\sqrt{Hz}})\times(32e3)\sqrt{\frac{\pi}{2}\times 1e6} = 120(\mu V)$$

$$V_{n\_Total} = \sqrt{V_{eno}^{\;2} + V_{eT(Rf)}^{\;2} + V_{ino}^{\;2}} = \sqrt{(73.4)^2 + (28.4)^2 + (120)^2}(\mu V) = 144(\mu V)$$

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Here are the calculations based on an example to show how the noise is integrated over the noise gain. Here, the noise gain is assumed to have a single zero at 100KHz and the pole at 1MHz is ignored for simplicity. The noise density (nV/√Hz) function is multiplied by the noise gain magnitude and then squared before being integrated over the total range (0Hz to 1MHz).

The other simplifying assumption made is that the op amp noise voltage is constant over the entire range. This is not a bad assumption since the contribution of the 1/f region of the op amp is negligible in a situation like this where BW reaches into the MHz region.

As far as the input noise current (in) is concerned, there is only a single pole located at fp. The same is true for the RF noise voltage which sees a single rolloff at fp .

The resultant noise voltage from all sources is then summed together in a square root of the sum of the squares fashion before arriving at the total rms output noise (V).

It turns out that the dominant noise source would be the op amp input noise current. The op amp input noise current is given by: √(2qIb), where Ib is the input bias current. Therefore, it's obvious that choosing a device with minimal input bias current would be advantageous in terms of noise.

Optimization Guidelines

•Op Amp: the voltage noise and the current noise times Z_D should both be as small as you can get. If one of these noises is much larger than the other, then you're probably far off optimum. Lower input capacitance also helps to reduce the noise gain peaking effect. Noise is reduced by the square root of the BW.

•Photodiode: If you have a choice, choose one with low capacitance (at the expense of sensitivity). This would reduce noise gain peaking.

•R_F: A lower resistor value decreases resistor noise as a function of $\sqrt{(R)}$, but it also lowers the desired I-V gain as a direct function of R. Therefore, lowering R reduces the SNR at the output. The feedback resistor should be as large as possible to maximize SNR.

C_F: The noise contribution due to R_F can be decreased by raising the value of C_F (lowering f_p) but this reduces signal bandwidth.

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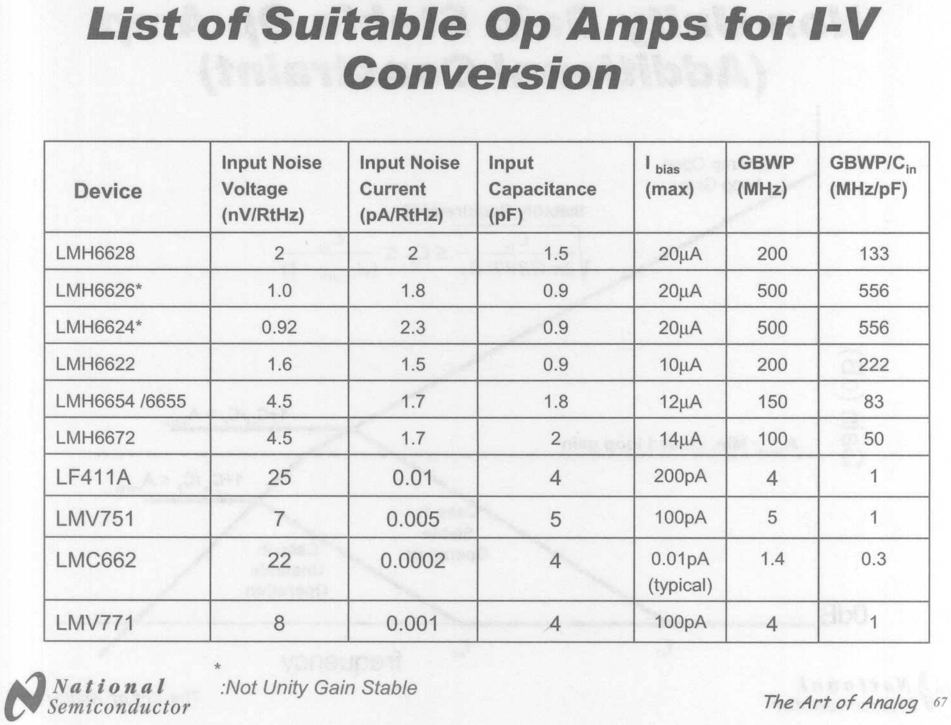
For the op amp noise voltage, the highest noise contribution comes at the highest frequency ranges. Therefore, to calculate Zd (diode impedance), use the highest frequency of interest. As Zd decreases, the voltage noise becomes more dominant and vice versa. Therefore, the voltage and current noises can be conveniently and simply compared in this fashion.

As far as the diode capacitance is concerned, it is interesting to observe that if Cd is lowered, the noise gain peaking effect is reduced. This could have a very significant effect on the overall noise without effecting the BW. That is precisely why it's important to keep the total input capacitance low. On the other hand, increasing Cf would counteract the noise gain peaking at the expense of BW. The value of Cf is often times a compromise between the required BW and the noise gain.



List of Suitable Op Amps for I-V Conversion

Device	Input Noise Voltage (nV/RtHz)	Input Noise Current (pA/RtHz)	Input Capacitance (pF)	I_{bias} (max)	GBWP (MHz)	GBWP/C_{in} (MHz/pF)
LMH6628	2	2	1.5	20µA	200	133
LMH6626*	1.0	1.8	0.9	20µA	500	556
LMH6624*	0.92	2.3	0.9	20µA	500	556
LMH6622	1.6	1.5	0.9	10µA	200	222
LMH6654 /6655	4.5	1.7	1.8	12µA	150	83
LMH6672	4.5	1.7	2	14µA	100	50
LF411A	25	0.01	4	200pA	4	1
LMV751	7	0.005	5	100pA	5	1
LMC662	22	0.0002	4	0.01pA (typical)	1.4	0.3
LMV771	8	0.001	4	100pA	4	1

*:Not Unity Gain Stable

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The Art of Analog 67

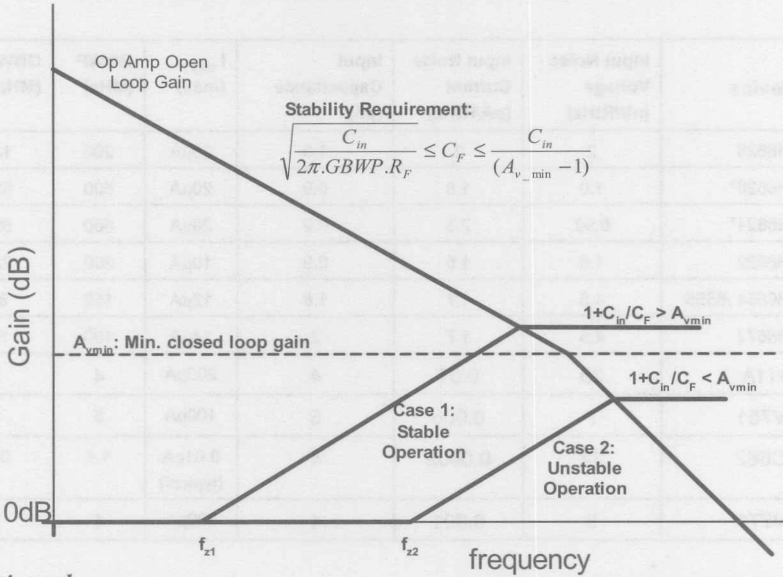
For current feedback Op Amps, the inverting current noise is usually much higher than that of the non-inverting input. Therefore, as far as noise is concerned, the CFA is not the best choice. All devices listed here are of the voltage feedback topology.

When considering the choice of device to be used, a rough measure of max possible I-V bandwidth would be the ratio of GBWP/Cin.

If ultra low noise and maximum DC accuracy are important in your application, you could use some of the amplifiers shown here with input bias currents in the pA range (last 4 devices from the bottom). As you can see, reducing the input bias current means an automatic improvement in input current noise as well. So, you gain higher DC accuracy and reduced noise at the same time!

In addition, the LMC662, LMV751, & LMV771 also allow input common mode voltage to extend below V-; this makes for easier interface to the Photo diode and could allow easy adoption to single supply use. The LMV751 & LMV771 could also allow usage down to very low supply voltages (2.7V).

Non-Unity Gain Stable Op Amp (Additional Constraint)


Op Amp Open Loop Gain
Stability Requirement:
Gain (dB)
A_{vmin}: Min. closed loop gain
$1+C_{in}/C_F > A_{vmin}$
$1+C_{in}/C_F < A_{vmin}$
Case 1: Stable Operation
Case 2: Unstable Operation
0dB
f_{z1}
f_{z2}
frequency

$$\sqrt{\frac{C_{in}}{2\pi.GBWP.R_F}} \le C_F \le \frac{C_{in}}{(A_{v\_min}-1)}$$

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The Art of Analog 68

Devices which have a minimum closed loop gain requirement (i.e. LMH6624 & LMH6626) need special considerations when it comes to stability. These devices are optimized to provide maximum possible speed for the amount of power they use. In the case of the LMH6624 & LMH6626, the minimum closed loop configuration is 10V/V (20dB). In the I-V converter configuration, there is the additional constraint of increasing Noise Gain which gives rise to further phase shift which must be accounted for.

To ensure stability, the following must hold true:

$1+C_{in}/C_F >=10$ (this is dictated by the op amp's minimum closed loop gain). This can be simplified to $C_F<=C_{in}/9$

$C_F >= \sqrt{[C_{in}/(2\pi.GBWP.R_f)]}$ (this is dictated by the feedback characteristics discussed earlier).

IF the conditions above can be met simultaneously, the preferred value for C_F from a BW point of view would be the smaller of the two which is dictated by the feedback function (C_{in}, R_F, GBWP).

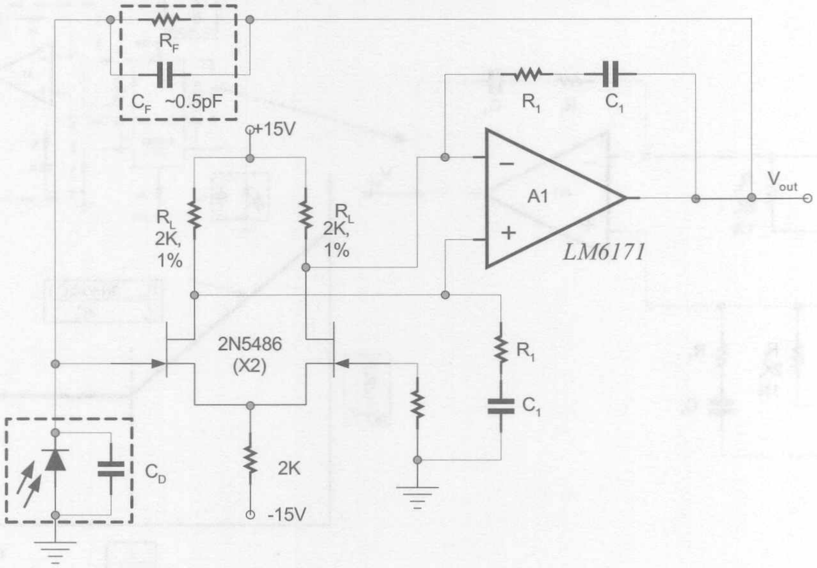
Therefore:

$\sqrt{[C_{in}/(2\pi.GBWP.R_f)]} < C_F < (C_{IN}/9)$

For the specific case of the LMH6624 & LMH6626, because of the large GBWP of these two devices, in almost all cases the solution exists. There will be a value of C_F which satisfies both conditions as long as:

$C_{in} >= 25.8e\text{-}9/R_F$. In other words, with a nominal value of 20pF for C_{in}, the minimum trans-impedance gain would be 1200V/A or else the circuit would be unstable.

Composite I-V Converter



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The Art of Analog 69

As we found earlier, the input noise current could have a profound effect on overall noise, especially with large Rf. Here is a neat way to optimize the I-V converter.

The choice of good low-noise JFET's on the input eliminate input noise current as a contributing factor.

Here are the advantages of this composite amplifier over a simple op amp circuit:

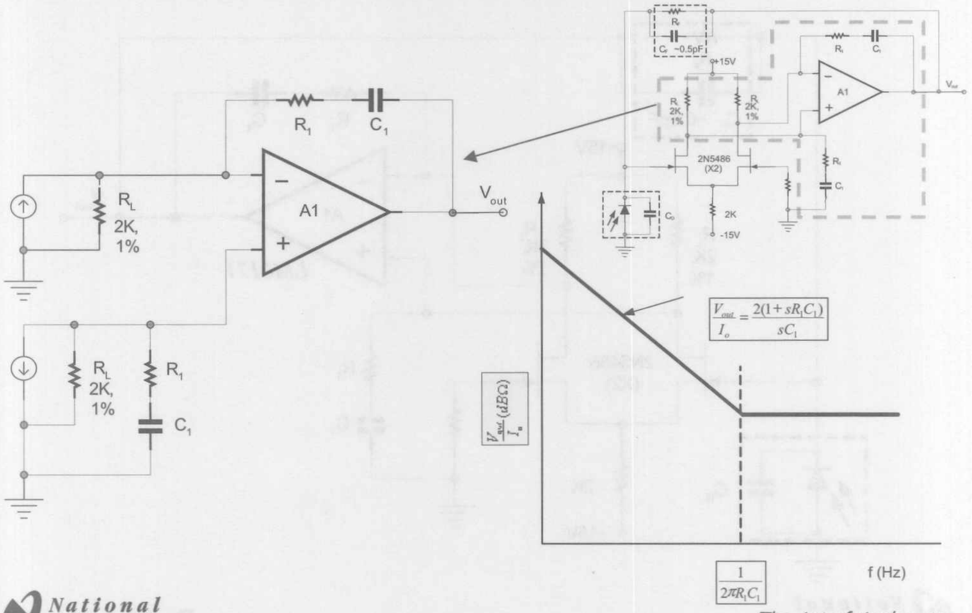
-Input differential pair tail current can be substantially increased to reduce input noise voltage.

-Input noise current would reduce significantly because of the FET's extremely low bias current

-By proper selection of compensation components R1 and C1, one could alter the open loop response to ensure stability. This is in contrast to the method discussed earlier which required increasing R_F, since this method would ultimately limit BW but R1, C1 setting won't.

When configured as shown, the noise requirements on the A1 are eased. The differential pair on the pair becomes the dominant factor in the overall noise. A good general purpose Op Amp such as the LM6171 would work well here allowing operation with +/-15V supplies thereby getting maximum dynamic range.

Composite I-V Converter Analysis



$$\frac{V_{out}}{I_o} = \frac{2(1+sR_1C_1)}{sC_1}$$

$$\frac{1}{2\pi R_1C_1}$$

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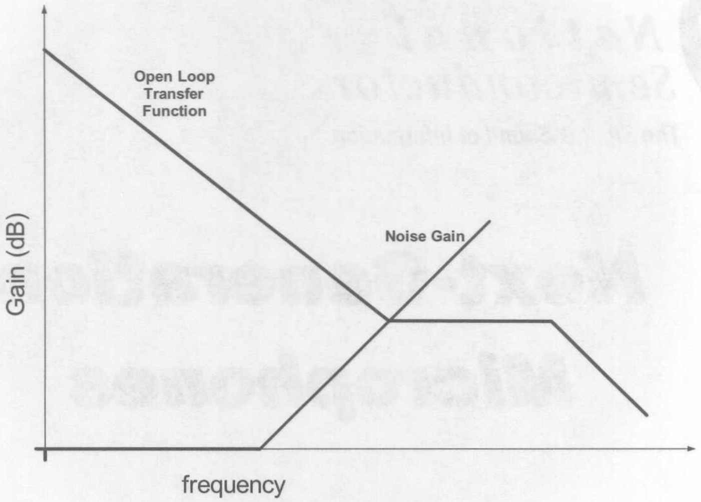
The Art of Analog 70

This is the schematic of the gain stage inside the composite amplifier shown on the previous slide. The schematic of the shaded area is isolated and shown on the left hand side. The current out of the JFET differential pair is shown as I_o. To the right is the bode plot of the transfer function to Vout. In contrast to what has been discussed so far, this amplifier configuration allows the open loop gain response to be reshaped as opposed to the feedback factor (ie using C_F across R_F). The open loop gain of the previous page's schematic is shaped using the R1, & C1 placed inside the loop. Using 1% precision load resistors for the two load resistors (2Kohm), the open loop gain becomes a function of R1, & C1 only.

Shaping the Open Loop Gain Curve



The composite amplifier just discussed could be made to have an open loop response resembling that shown here by the proper selection of R1, and C1. As can be observed on this plot, the noise gain and the X curves intersect each other at a point where the phase shift around the loop is 135 degrees (Phase margin of 45 degrees). Note that the useable BW did not have to be sacrificed to ensure adequate phase margin in this case.

At the point of intersection, that is when loop gain is 0dB, the signal has already gone through 180 degrees of phase shift had there not been a zero in the open loop transfer function. The presence of this zero adds 45 degrees of phase lead around the loop resulting in 45 degrees of phase margin.

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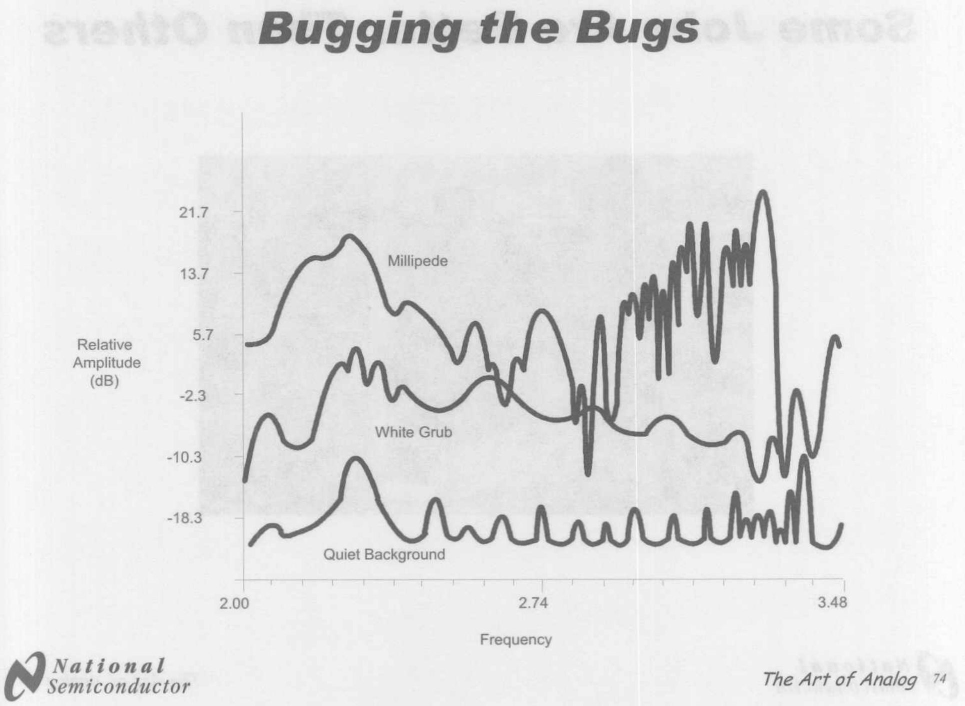
The Sight & Sound of Information

Next-Generation Microphones

Some Jobs Are Better Than Others

What are these men doing? They are orchard workers sifting through piles of dirt while sitting under the hot Florida sun. Why? They are listing and counting the insects present in the soil around their fruit trees to determine the level of pest damage that is likely. From this they can decide the amount and severity of the pesticides needed to protect the trees.



Bugging the Bugs

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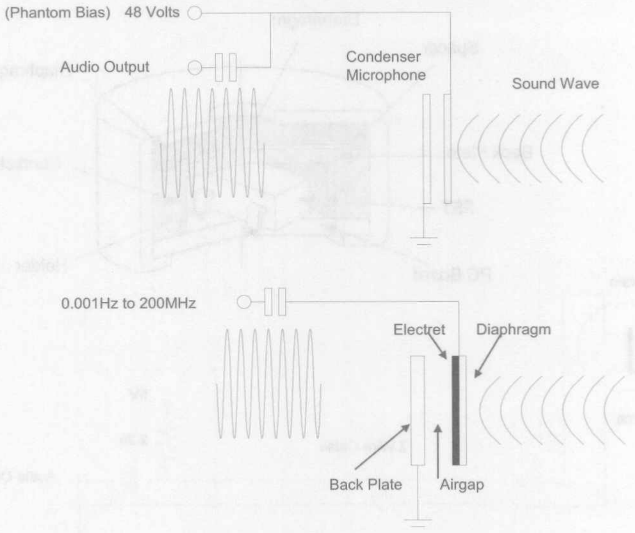
The Art of Analog 74

Researchers for the USDA Agricultural Research Service have found that electret microphone elements can provide acoustic signatures for various pests, such as the wheat stem sawfly and weevils, that attack the roots of orange trees. Under reasonably quiet conditions these pests have been detected within a few seconds at distances up to 30cm with 100% accuracy. Even under adverse conditions (high winds or local vehicular traffic) the accuracy is still at least 74%. Other researchers have recorded the Lemon tree borer larva (Oema herta), giving a non-destructive method of detecting borers prior to treatments for infestation.

Electret microphones, the name is said to come from the words *electric magnet*, are the most widely used type of microphones today and it has been estimated that current production is over a billion units a year. Apart from eavesdropping on insects, electrets are used in cell phones, hearing aids, cameras, computers, bat detectors, echo locators and even in high end studio audio. It is unlikely that a day will go by without you coming into contact with, or using, an electret microphone.

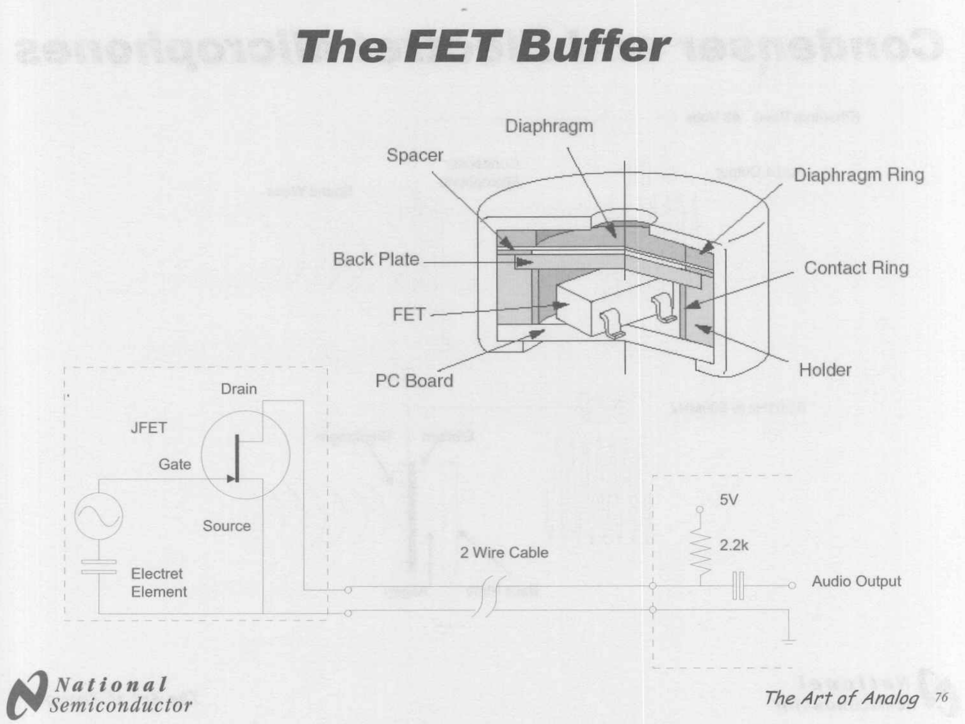
Electrets are inexpensive to manufacture, can be made physically very small, yet are rugged and can offer extremely high fidelity.

Condenser and Electret Microphones



Electret microphones are similar in operation to condenser microphones (and are commonly known as ECMs, or Electret Condenser Microphones) where two parallel plates of thin metal are mounted close to each other. A high dc voltage (c. 50V) is applied across the plates to polarise them with a constant charge. When sound waves impact the plates they flex slightly causing a change in capacitance. This change in capacitance produces an ac voltage with a frequency and amplitude proportional to the sound wave. The electret differs from the condenser microphone in that it does not require the high phantom bias voltage to establish the charge on the plates.

In the late thirties and early forties researchers found that a thick layer of wax material uniformly spread over a thin flexible diaphragm could hold a more or less permanent charge. This electret meant that high bias voltages were not required during use of the microphone elements. Modern electrets are based on the work done by West and Sessler of Bell Labs in the 1960's. They found that a thin foil of teflon dielectric material would hold a permanent charge which, when applied to a diaphragm, established an electric field in the small air gap between the diaphragm and a closely mounted back-plate. Microphones with the electret attached to the diaphragm are known as front electrets. More recently, the electret is applied to the back-plate, (back electrets), allowing thinner (and more flexible) diaphragms to be used. Thin polymer electrets have extended the frequency range from 10^{-3} Hz to over $2x10^8$ Hz.



The FET Buffer

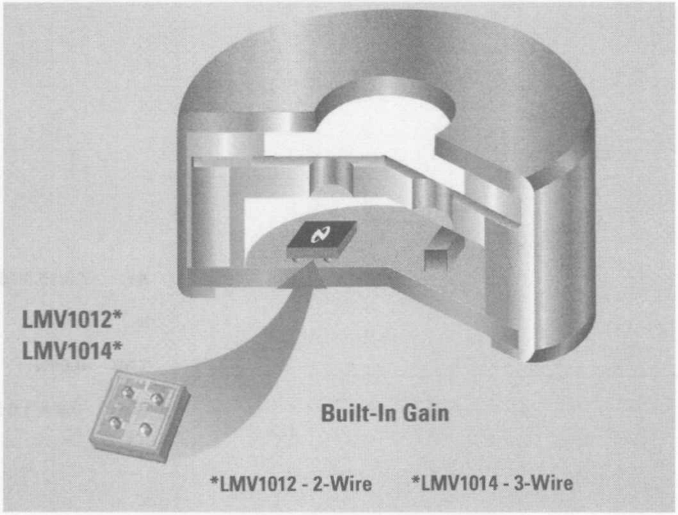
The electret element has a very high impedance and this presents problems in coupling the microphone output to subsequent amplifier stages, particularly if these amplifiers are at the other end of a cable. To a large measure this has been solved by using JFETs to buffer the element and present a relatively low impedance to the cable, as shown above. Although the JFET requires a dc bias voltage, the standard two wire cable is still used, with the bias source at the other end of the wire carrying the signal output. This is not phantom power in the sense applied to condenser microphones, and is usually a much lower voltage, from 1V to around 9V. The microphone impedance is related to the size of the bias resistor and is most often in the range of 2 kΩ to 5 kΩ.

An important factor in the development of electret microphones is decreased size. Early JFET ECMs were quite large in order to accommodate the JFET packages, but now JFET packages as thin as 0.5mm are commonly available and the total ECM thickness is as small as 2mm.

Along with small size the JFET confers additional benefits, particularly in telephony applications. The gate impedance of the JFET, along with the capacitance of the microphone element forms a low pass filter with a cut-off frequency around 100Hz. This helps to attenuate large low-frequency signals such as wind noise or breath noise with close-in speakers. The gate is a reversed-biassed diode connected across the capacitive signal source. Leakage current in the gate diode ensures that the gate voltage is close to 0V. Very large overdriving signals are clipped by forward conduction of the diode and the reverse leakage current.

While the JFET buffer has benefits, it also has disadvantages. The output signal is developed across the load resistor that is also supplying the current to the JFET. This means that the JFET will have low gain and the ECM will have low sensitivity. The spread in gate threshold voltage means that there will be a large variation in the supply current drawn by the ECM, from 200uA to over 800uA, and the THD will be in the range of 1 to 10%.

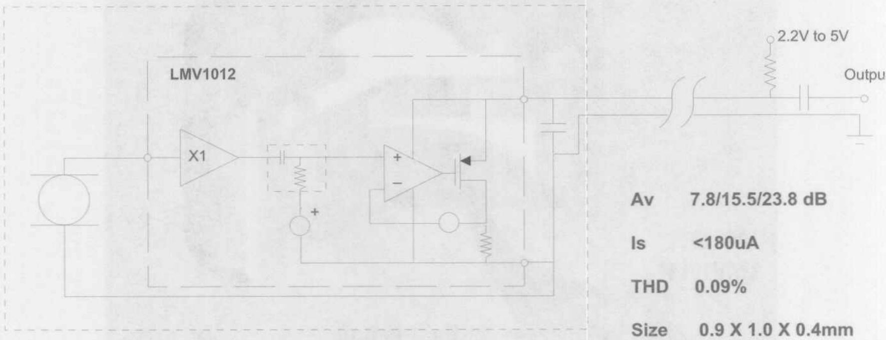
Next-Generation Electret Condenser Microphone



While JFET packaging developments have made it possible to produce ECMs with very small form factors, very little has been done to improve the sensitivity and lower the THD of the buffer amplifier. Efforts to replace the JFET have met with limited success….until now.

Utilizing experience in designing and manufacturing small, low power consumption operational amplifiers, National is introducing a new range of pre-amplifiers intended for use with electret microphones, both 2-Wire and 3-Wire, with improved performance over their JFET equivalents.

Integrated 2 Wire ECM



Av	7.8/15.5/23.8 dB
Is	<180uA
THD	0.09%
Size	0.9 X 1.0 X 0.4mm

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The Art of Analog 78

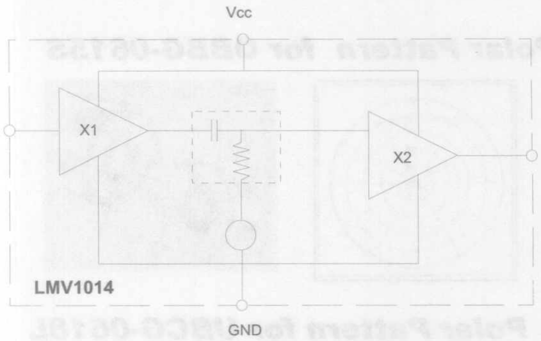
Overcoming the JFET's disadvantages with an integrated pre-amplifier while retaining the benefits and still remaining low cost can be quite challenging. High-input-impedance amplifiers are readily available but the smallest of these are typically in five lead packages with a package thickness of 1.1mm.

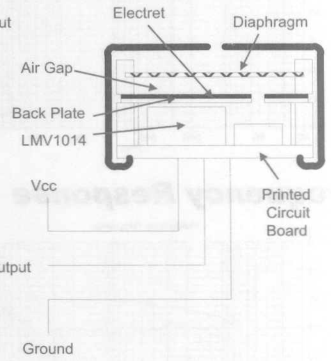
In 1999 National introduced the chip scale package, known as micro SMD, which is now available with dimensions of 0.93 X 1.0 X 0.4mm. Since the introduction of the micro SMD package, we have designed and manufactured a number of low-voltage, low-power amplifiers using a BiCMOS process. CMOS devices have near ideal high input impedances (>1000GΩ) but, unlike a JFET, the input stage requires biassing for linear operation and help with recovery from input overloads. In the LMV1012 this bias is provided by back to back diodes which also make a fast recovery circuit for the input MOS follower. Large, low frequency signals are attenuated by an internal high pass filter before the signal is passed on to the high-gain output stage. The filter also provides a convenient point to dc bias the output stage to approximately half the nominal supply voltage for maximum output dynamic range. To replicate the two wire output of the JFET ECM, a transconductance stage sets a current flowing through the load resistance. Since the output node is the supply rail, RF signals on the supply rail can be coupled into the circuit. Most ECM manufacturers add small by-pass capacitors (20-30pF), but careful layout of leads from the microphone are still required.

Signal voltages from the electret* are of the order of 100uV to 10mV on average, with 100-130mV peaks. The LMV1012-15 has a set gain of 15.5dB to avoid clipping on high signal swings. Higher (23.8dB) or lower (7.8dB) gains are available with the LMV1012-25 and the LMV1012-07 respectively. All three devices feature THDs of 0.1% and SNRs of 60dB.

*OBBG 0615S/0622S from BSE (www.bsecm.com)
Best Sound Electronics
#869-3, Jacjun-1dong
Keiyang-ku, Inchon-si, South Korea.

3-Wire ECM





Is	**38uA**
PSRR	**88dB**
Zo	**<200Ω**
Vcc	**1.7V to 5V**

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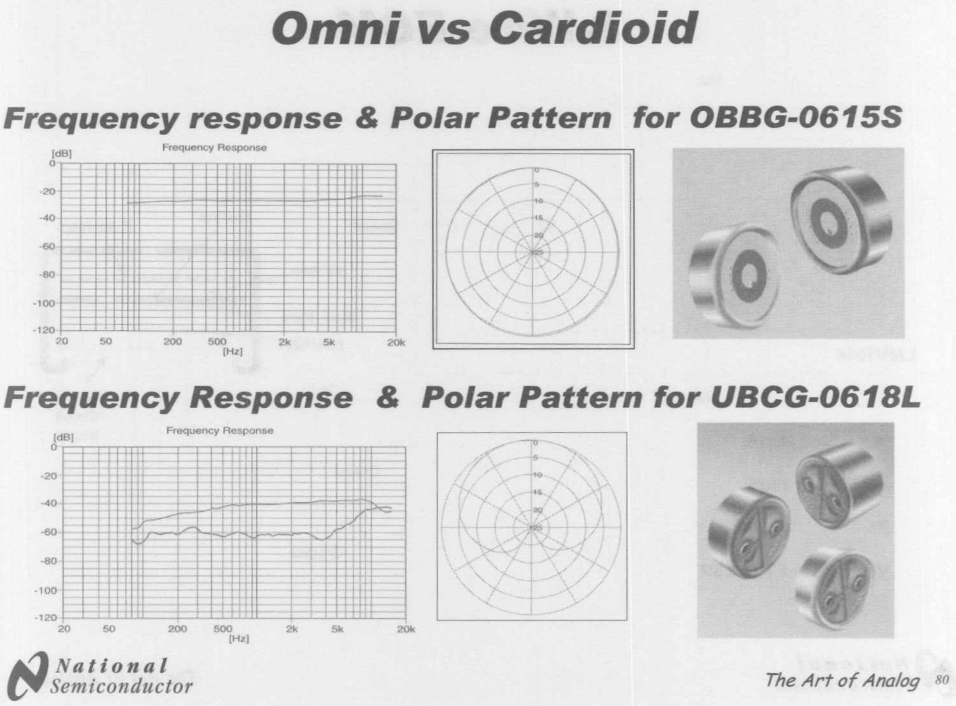
The LMV1012 is designed as a direct replacement for the conventional JFET ECM. With the same form factor, replacement involves simply substituting the microphone elements. Immediate benefits are improved sensitivity, lower distortion and lower supply currents (total supply current with 2.2KΩ loads are 160uA for the LMV1012-07 and LMV1012-25, and 200uA for the LMV1012-15).

Some battery-powered applications (Bluetooth™ technology) need even lower supply current levels, and if a 3 wire interconnect to the ECM is permissible, a more conventional output stage, such as that used by the LM1014 can be employed. Separating the output lead from the supply current lead means that high PSRRs can be readily achieved (88dB) with a much lower total supply current (38uA) for comparable noise levels. Although the PSRR falls off above 1kHz, it is still good enough to handle the GSM modulation rate of 216 Hz and its harmonics. RF decoupling capacitors may still be required on the supply line, but the lower output impedance of the LMV1014 (<200Ω) makes the signal output less susceptible to noise pick-up.



Omni vs Cardioid

Frequency response & Polar Pattern for OBBG-0615S

Frequency Response & Polar Pattern for UBCG-0618L

The Art of Analog 80

An omnidirectional microphone has an equal response to sound waves coming from all directions. A cardioid microphone, sometimes called a noise-reducing microphone, has reduced response to sound waves that are off-axis. Note that this is a decreased response, not an enhanced response to on-axis signals.. Because the off-axis response to ambient noise is less than that for an omnidirectional microphone, the cardiod is said to have a distance factor. For example, a distance factor of 1.8 means that the cardioid will have the same signal to ambient noise ratio at 18 inches as will the omnidirectional at 10 inches. Cardioids will also exhibit a proximity effect. When the speaker is close in to the microphone, frequencies below 500Hz get boosted compared to frequencies above 500Hz. This means that a voice can sound richer and deeper close to the microphone, but thinner and reedy further away from the microphone.

References

0dB SPL smallest sound normally detectable (20µPascals)

60dB SPLNormal speech at 3 feet distant

70dB SPLBusy Traffic

74dB SPLNormal speech at 1foot distant

94db SPL Normal speech at 1 inch distant (1 Pascal=10µbars=10dynes/cm^2)

Electret Microphone Sensitivity = -44dB SPL = 6.3mV

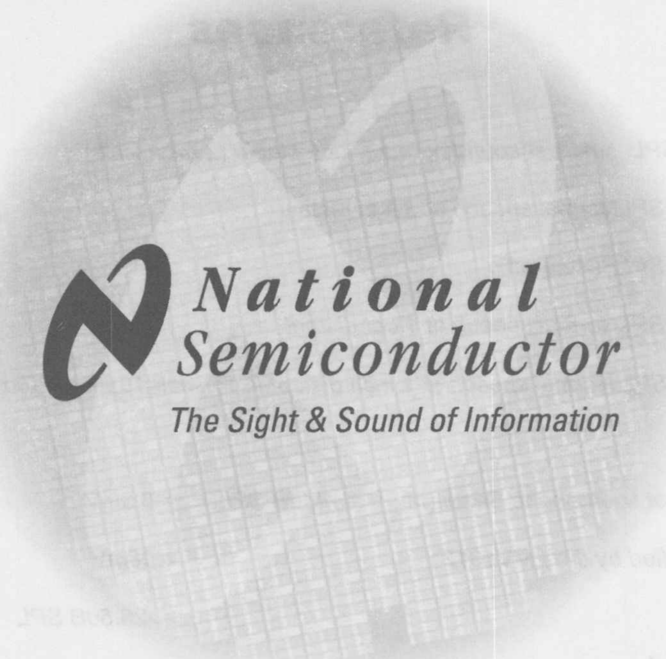
Amplified by the LMV1012 = 38mV

= -28.5dB SPL

On the previous page, the frequency response for each microphone element was plotted with respect to relative amplitude …….. relative to what? Unfortunately, microphone manufacturers and the makers of electronic amplifiers have their own favourite reference levels and you need to know the relationship in order to make comparisons of specifications between different microphones. For the amplifier it is useful to know the microphone sensitivity in dB relative to 1 Volt (dBV), or for professional audio equipment in dB relative to 0.775 Volt (dBu), in order to determine if the amplifier noise floor will affect the overall S/N ratio. For the microphone manufacturer it is more useful (for comparative purposes) to know the sensitivity relative to sound pressure level (SPL).

0dB SPL (20µPa) is considered to be the smallest detectable sound level but this is not the reference level used for the microphone sensitivity specification. Instead either 74dB SPL or 94dB SPL are used as references. 74dB SPL is the sound pressure generated by normal speech at 1ft from the microphone. 94dB SPL is the sound pressure for normal speech within 1in of the microphone and corresponds to 1 Pascal = 10 µbars = 10 dynes/cm2. The reference voltage level is 1V/Pa. For example a microphone element with a sensitivity of -44dB SPL relative to 1V/Pa will generate a voltage of 6.3mV. Amplified by an LMV1012-15 this will give a microphone output level of 37.8mV or –28.5dB SPL.

Microphone noise measurements are given either as a SNR (dB) ratio or as a voltage referenced to 1V (dBV). It is not always clear which one is being used and the measurements are invariably A-weighted. This comes from the early days of telephony where measurements were made through a band-pass filter centered at 2-3kHz with a sharp rolloff on either side, -10dB at 20kHz and –20dB at 100Hz. A-weighting usually improves the measured S/N by 3dB to 6dB over an unweighted measurement.



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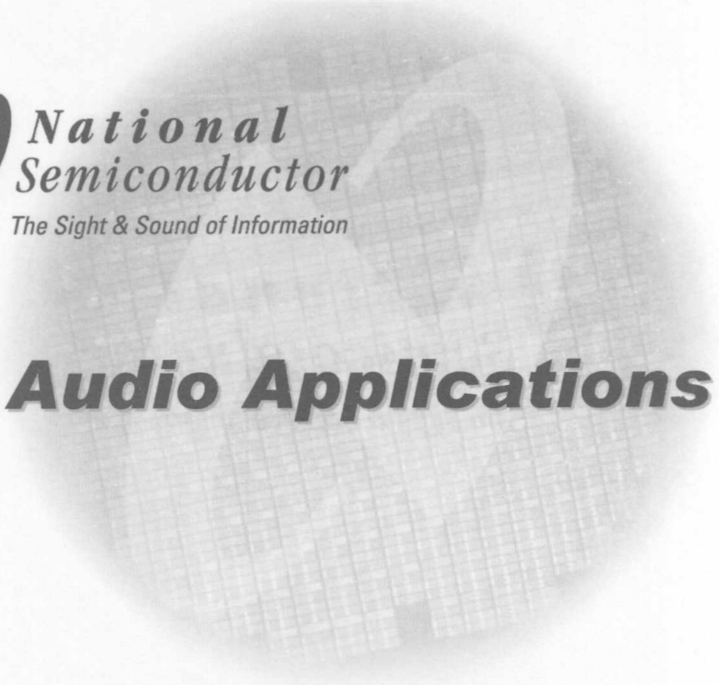

Audio Applications

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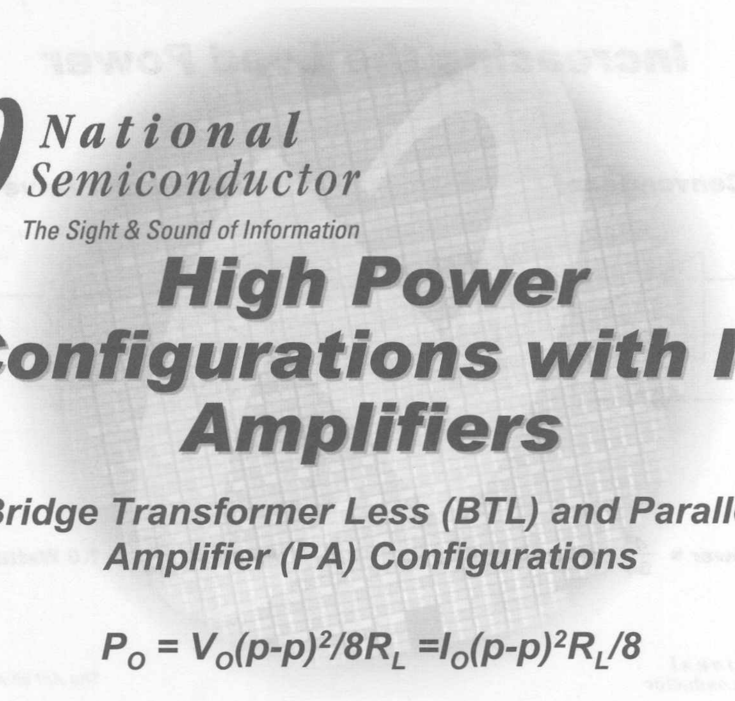


High Power Configurations with IC Amplifiers

Bridge Transformer Less (BTL) and Parallel Amplifier (PA) Configurations

$$P_O = V_O(p\text{-}p)^2/8R_L = I_O(p\text{-}p)^2R_L/8$$

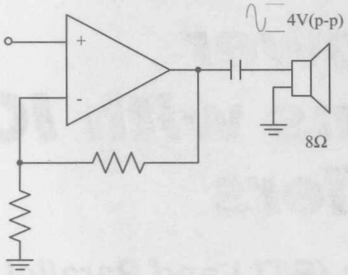
The maximum amount of ac (sine wave) power that can be delivered to a given resistive load RL is limited either by the maximum voltage swing available from the amplifier output or (less likely) the maximum current swing the amplifier can deliver. The interdependence of these quantities is illustrated by the simple expressions given below where VO(p-p) is the output voltage swing and IO(p-p) is the output current swing.

$$\text{Power} = VO(p\text{-}p)^2/8RL = IO(p\text{-}p)^2RL/8$$

For most audio amplifiers, voltage swing is largely dependent on the supply voltage or the semiconductor process breakdown voltage, whichever is lower. For a given load the maximum current (and output power) is determined by this voltage swing. The amplifier current capability usually depends on the design topology and the size of the output transistors. Normally I/C audio amplifiers are designed with specific loads and supply voltages in mind, but when an audio system designer wants more power but is constrained by a (lower) supply voltage, conventional approaches do not always work.

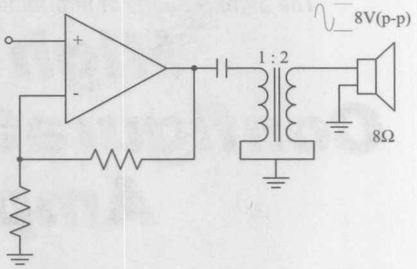
Increasing the Load Power

Conventional



$$\text{Power} = \frac{4^2}{64} = 0.25 \text{ Watts}$$

Transformer Drive



$$\text{Power} = \frac{8^2}{64} = 1.0 \text{ Watts}$$

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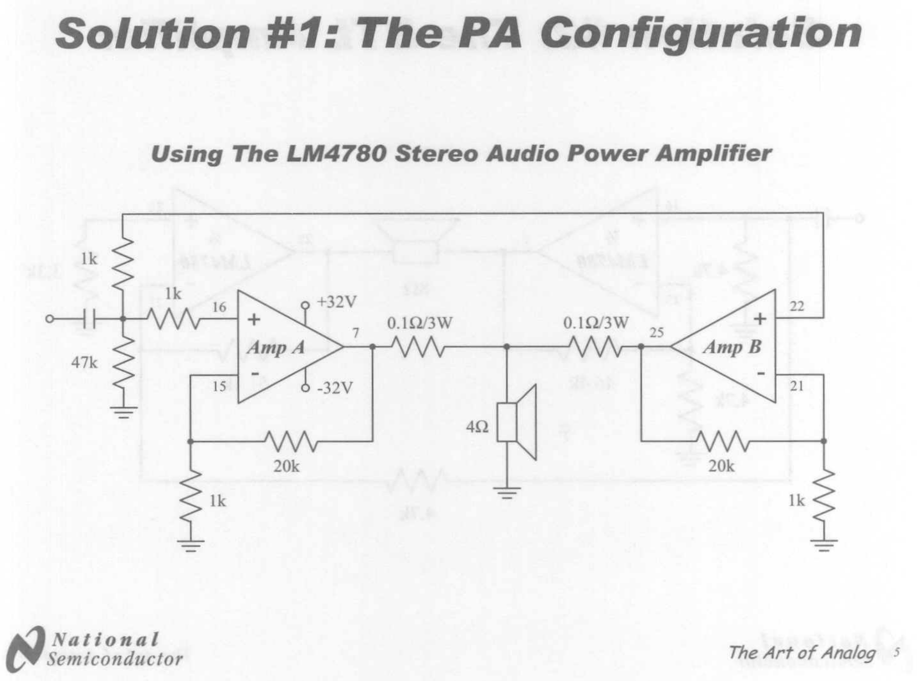
The Art of Analog 4

The introduction of portable entertainment equipment was one of the earliest trends that made working with low supply voltages voltages important, and many transistor radios used transformer coupled speakers. As shown here, even a modest turns ratio of 1:2 will double the swing across the loudspeaker with a four times increase in power. Unfortunately, particularly when much higher power outputs are required, the expense, bulk and radiated field of the transformers start to make this approach unattractive. Also, note that in the example above, the load presented to the amplifier is increased by the square of the turns ratio, to 2Ω instead of 8Ω, and the amplifier has to deliver peak currents that are four times higher. Nothing is for free, and the higher output power is achieved at the expense of higher amplifier internal power dissipation.



Solution #1: The PA Configuration

Using The LM4780 Stereo Audio Power Amplifier

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The Art of Analog 5

The low cost and ease of use of modern high power audio amplifiers make it very practical to apply different topologies to replace transformer drive.

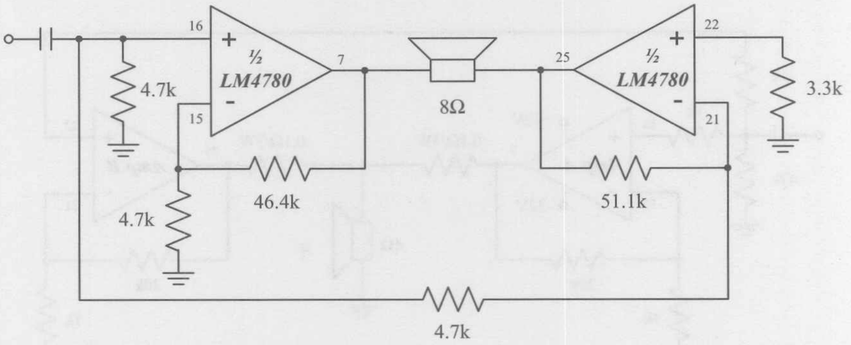
Where the amplifier and speakers are provided together to make a complete system, the speaker impedance can be lowered to 4Ω or even 2Ω to get the required increase in power output. Nevertheless, on large systems, the increased current to drive these loads can easily cause excess power dissipation in the power amplifier, or the peak current can actually exceed that available from the amplifier output transistors. A solution to this problem is to employ two similar amplifiers connected in parallel across the speaker.

In the case of a 4Ω load, each amplifier is matched in gain (use 1% resistors to set the gain) and so delivers only half the load current required for the speaker. As far as each amplifier is concerned, the effect is the same as driving an 8Ω load, so the internal peak current and power dissipation are the same as for an 8Ω load, yet the power output is actually into a 4Ω load.

To further ensure good matching between the amplifiers, dual amplifiers, such as the LM4780, are easily available. This power amplifier is a new Overture® series two channel amplifier, the LM4780, which can deliver 60 Watts/channel into 8Ω loads. These amplifiers also feature a smooth transition fade in/out mute. They are available in 27 pin TO-220 style packages with a package θ_{JC} of 0.80C/Watt. The design shown here can deliver 100 Watts into a 4Ω load on 32V supply rails. This is 2X the power that could be delivered to an 8Ω load with the same power supply voltage.

Note: While dual, or stereo, amplifiers can solve the matching and output current requirements, since both amplifiers are in the same package, the total internal power dissipation will be the same as for a single amplifier driving the actual 4Ω load. Where dissipation and heat sinking remain an issue, two physically separate amplifiers should be used. In that case the power dissipation per amplifier is the same as that for an amplifier driving an 8Ω load.

Solution #2: The BTL Amplifier



When both terminals of the speaker are available (one side is NOT connected to ground) another approach is available, also using a dual amplifier in place of a single. While there are a number of different ways to connect the BTL or Bridged Transformer Less (also known as Bridge Tied Load) amplifier, all the ways will have one thing in common. In the absence of a differential drive source, one amplifier will be driven non-inverting, while the other will be driven inverting. The big advantage to this configuration is that the power output can be up to 4X that of an amplifier driving a single ended load from the same supply voltage.

In the absence of an ac signal the outputs of both amplifiers will be at the same potential, in this case 0Vdc, and the load is connected between the outputs. This means that the large coupling capacitor for a single-ended load has been eliminated. When an ac signal is applied and the output of the left hand amplifier swings positive, the output of the right hand amplifier will swing negative by the same amount. Ideally the left hand amplifier output can swing almost to the positive supply rail so that the total positive swing across the the load is twice the positive supply voltage. Similarly the maximum negative swing across the load will be almost twice the negative supply voltage. Since the power delivered to the load is proportional to the square of the voltage swing across the load, the power is increased by almost 4X. The word almost is used because in the real world the amplifier output will not be able to swing all the way to the supply rail. Headroom is required for the output stage transistors and this can be several volts when low distortion is important.

Note: Although the load is 8Ω, as far as each amplifier is concerned it is driving a 4Ω load and power dissipation per amplifier should be calculated assuming RL = 4Ω.

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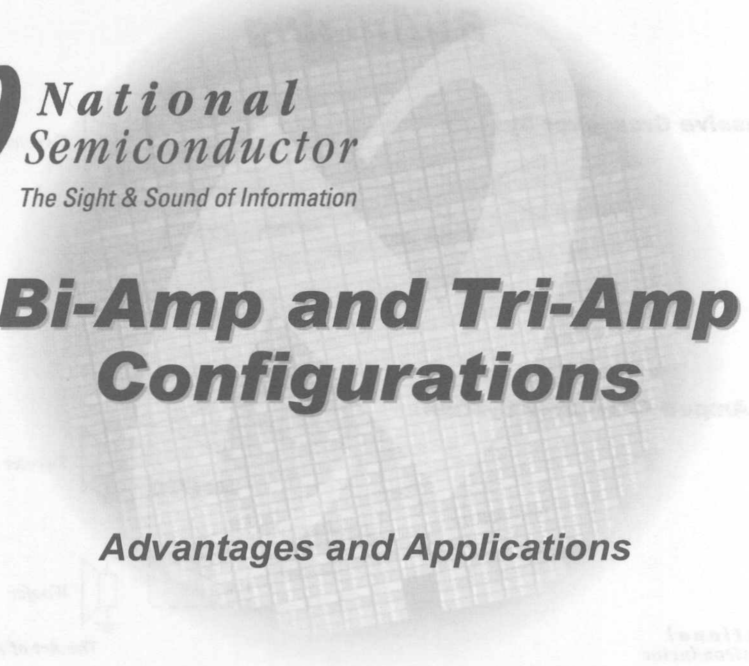
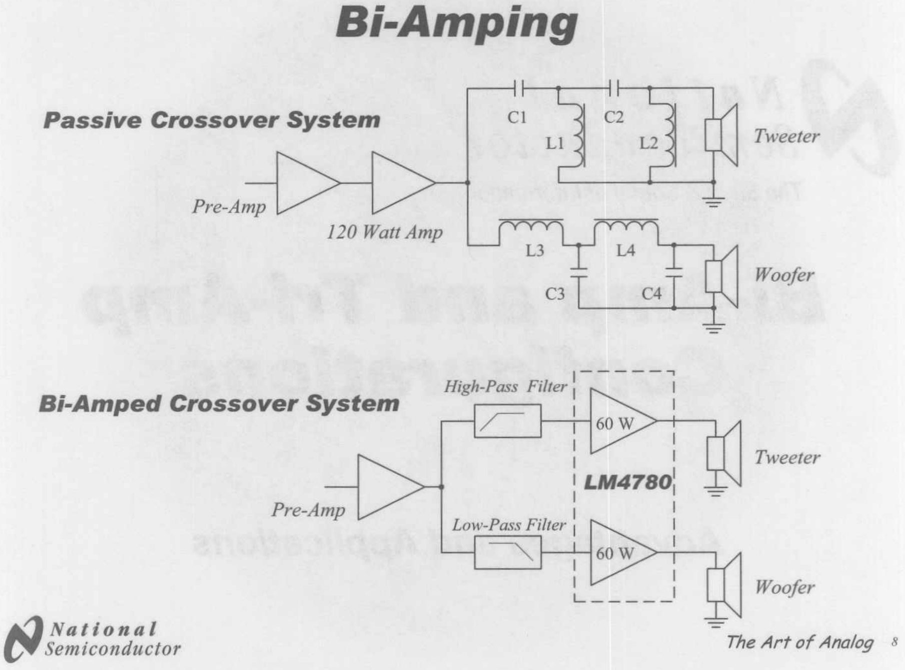


Bi-Amp and Tri-Amp Configurations

Advantages and Applications

Yet another solution to obtaining increased audio power is to provide separate amplifiers to drive each speaker in a loudspeaker enclosure. This is known as Bi-Amping or Tri-Amping.



Bi-Amping

Passive Crossover System

Bi-Amped Crossover System

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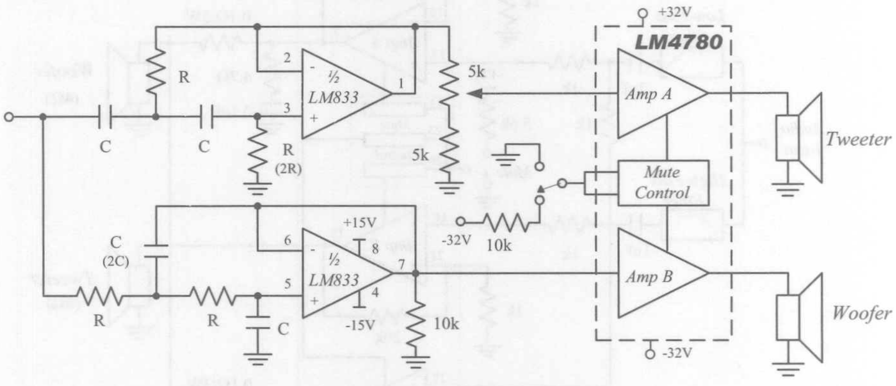
The Art of Analog 8

Because of the difficulty in manufacturing a single speaker capable of reproducing the entire audio spectrum, most Hi-Fi speaker enclosures have multiple speakers,where each speaker is designed to cover only one section of the frequency band. Since the power amplifier delivers the entire range of frequencies, separation of the audio signal is done with passive high-pass and low-pass filters, known as crossover networks. These networks have to handle high power levels and are composed of relatively large (and expensive) inductors and capacitors.

Crossover networks are difficult to design and even more difficult to tweak. They present a different load to the power amplifier than would be presented by the speaker alone and they consume power that would otherwise go to the speaker. Nevertheless, the presence of the crossover network inside the speaker enclosure means that almost any power amplifier designed to drive the nominal speaker impedance can be connected to any speaker enclosure with that impedance.

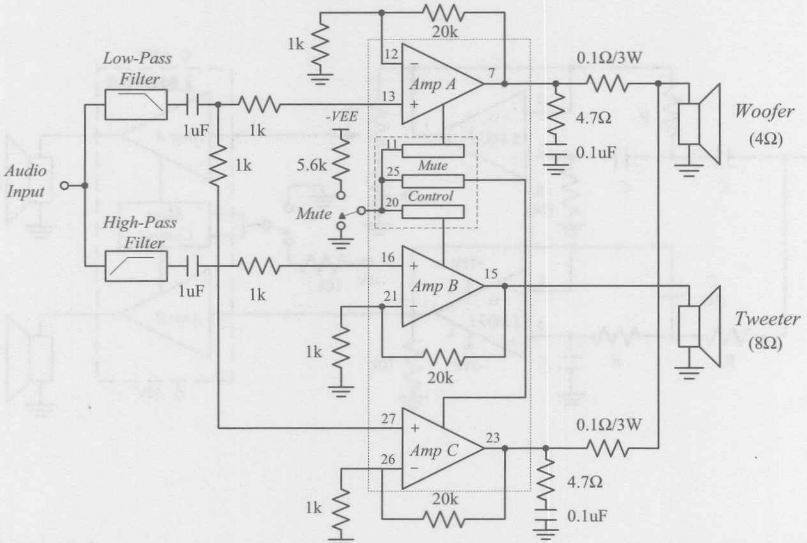
An alternative (for the go-it-alone audio enthusiast) is to provide separate power amplifiers for each speaker within the enclosure. In a bi-amp system one channel would handle the signals at the low end of the audio spectrum (the woofer), and a second channel would handle the signals at the high end (the tweeter). Separation of the signal frequencies occurs between the pre-amplifier output and the power amplifier inputs as shown above.

Bi-Amped LM4780 With Active Crossover Network



The audio signals passing through the crossover network are now line level signals from the pre-amplifier and the cumbersome passive networks can be replaced with active crossover networks. Here we are showing active 2nd order low-pass and high-pass filters using the LM833 dual audio amplifier. These filters are of the all pass type so the combined overall voltage response will be flat, and the crossover frequency Fc = 1/2πRC. Increasing the roll off rate in the stop band to 24dB/octave is done by simply cascading two 2nd order filters, the crossover frequency now being given by 1/2πRC√2. A quad op-amp, the LM837, can be substituted for the LM833 but lower power supply voltages will be needed. Notice that the output of the high-pass section has a trim pot to set the output level. This is because woofers have a generally lower efficiency than midranges and tweeters and the pot can be used to set up an overall acoustically flat response.

Bi-Amping With the LM4781



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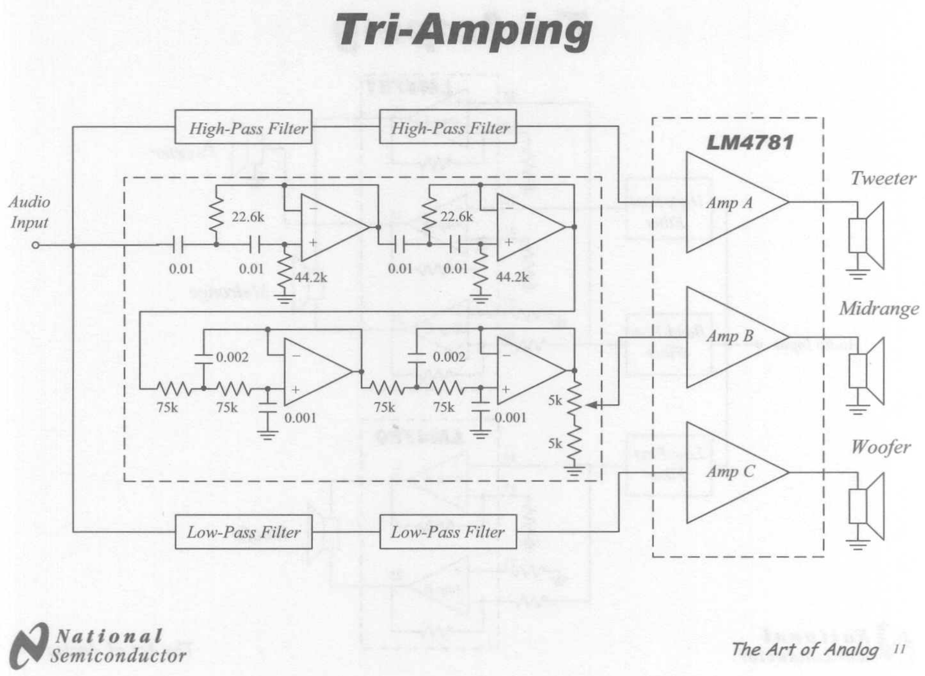
The Art of Analog 10

Although the audio frequency range is generally accepted to be between 20Hz and 20kHz, the energy in music signals is not evenly distributed over this range. In fact, for most music programmes, 70% of the energy occurs at frequencies below 700Hz. Less than 10% occurs at frequencies above 3.5kHz. This suggests that in a bi-amped system the woofer amplifier needs to be able to handle more power than the tweeter amplifier, or put another way, the tweeter channel needs less power than the woofer channel.

Shown above is yet another new Overture® amp, the LM4871. This is a three-channel amplifier, each amplifier capable of delivering 35Watts/channel into 8Ω loads. Here we are showing channels 1 and 3 driving the 4Ω woofer in parallel, and channel 2 driving the 8Ω tweeter.



Tri-Amping

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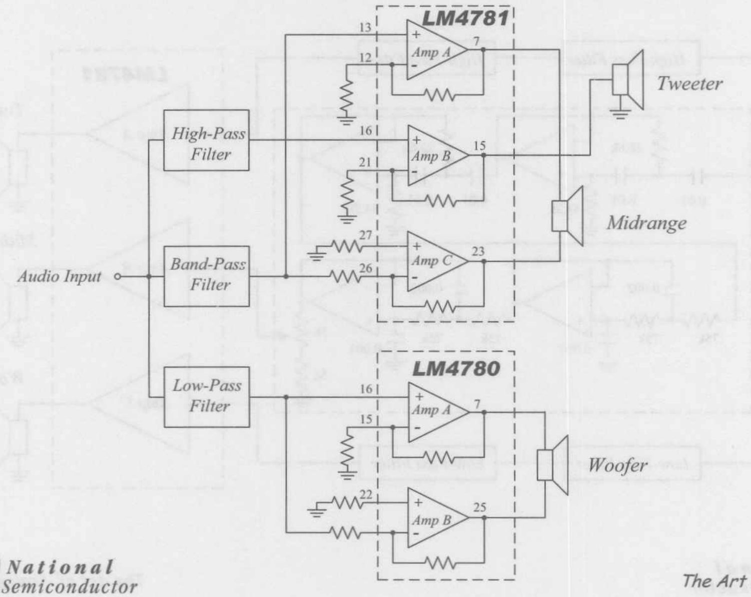
The Art of Analog 11

Three channel power amplifiers make it very easy to implement a three-way system. Now the audio spectrum is divided into three sections, a woofer amplifier driven through a low-pass filter, a midrange amplifier driven through a band-pass filter, and a tweeter amplifier driven through a high-pass filter. Although the crossover frequencies are different from the two-way system, the high and low-pass sections are designed as before, with the band-pass section formed by cascading a high-pass and a low-pass section.

Choosing the crossover frequencies depends on how adventuresome you feel. If the speakers come with a passive crossover, or are a matched set with recommended crossover frequencies, then you won't go too far wrong with staying with those frequencies. If you have the means to measure the individual driver characteristics, then go for it. In general terms the cone diameter is a good guide to the upper end of frequencies that the driver is good for. If the diameter divided by the acoustic wavelength at the highest frequency the driver is expected to reproduce with a flat response is less than or equal to 1, the crossover frequency will be in the right range. For a two-way system the crossover will be in the range of 800Hz to about 2kHz. A three-way system can have crossovers as low as 100Hz and as high as 4Khz. In the system shown here, fourth order filters are used with the component values in the filter network for crossover frequencies at 500Hz and 3kHz.

Using the LM4781 provides all the power amplifiers for a single three-way enclosure in one package, but does not take advantage of the reduced power requirements for the midrange and tweeter section.

Tri-Amping



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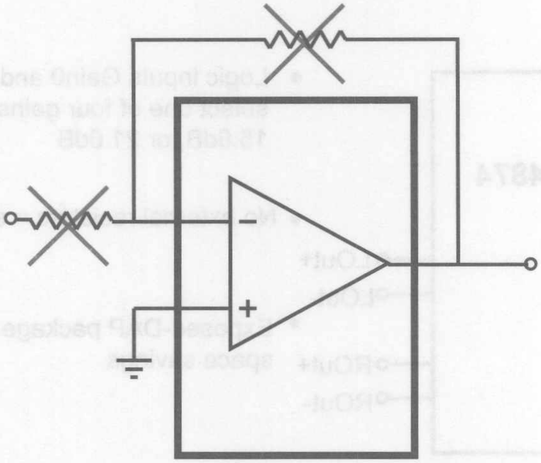
The Art of Analog 12

This design is a combination of the BTL and single ended configurations. The LM4870 is used to drive the woofer in BTL mode, amplifiers 1 and 3 of the LM4871 drive the midrange in the BTL mode, and amplifier 2 drives the tweeter in the single ended mode.

External Resistors Waste Board Space and Increase Cost



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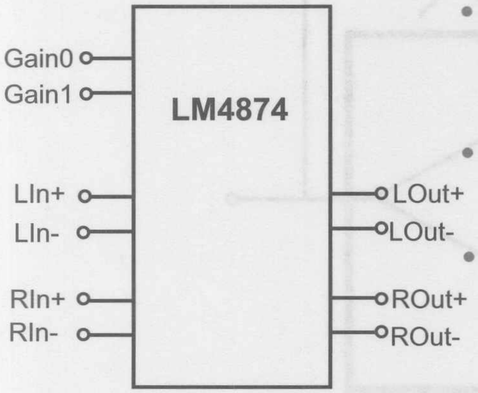
Many audio amplifiers require external resistors in order to set the gain. However, these resistors take up valuable board space and increase both cost and assembly time.

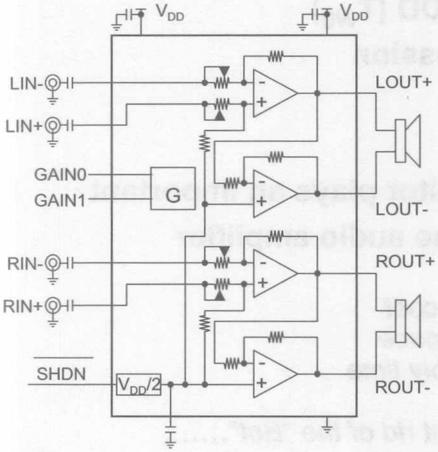
LM4874 – No External Gain-Setting Resistors Needed!



- Logic inputs Gain0 and Gain1 select one of four gains: 6dB, 10dB, 15.6dB, or 21.6dB
- No external resistors = space savings
- Exposed-DAP package – further space savings

The LM4874 provides a solution to these issues because its gain is set without any external resistors. The LM4874 features four fixed, internally set, BTL voltage gains: 6dB, 10dB, 15.6dB, and 21.6dB. Select one of the four gains by applying a logic level signal to the Gain0 (MSB) and Gain1 (LSB) digital inputs.

LM4874 – 2.1W Differential Input, BTL Output Stereo Audio Amplifier With Selectable Gain and Shutdown



- BTL Output Power of 2.1W ($R_L = 3\Omega$), 1.9W ($R_L = 4\Omega$), 1.2W ($R_L = 8\Omega$) [$V_{DD} = 5.0V$, THD+N = 1%]
- Micropower shutdown current = 0.1μA
- PSRR = 62 dB, at 1kHz, $V_{DD} = 5.0V$
- Exposed-DAP package – high thermal efficiency
- Applications: notebook computers, PDAs, portable electronic devices

The LM4874 also features pseudo-differential stereo inputs and BTL outputs. Operating on a single 5V supply, the LM4874 delivers 1.2W, 1.9W, or 2.1W of output power to an 8Ω, 4Ω, or 3Ω BTL load, respectively, with less than 1% THD+N. Other features include an active-low micropower shutdown mode input, thermal shutdown protection, and improved "click and pop" suppression. The LM4874 is designed for notebook and other handheld portable applications.

The Reference Bypass Capacitor:

- **Filters out noise on the input node**
- **Affects charging time to ½VDD (T_{WU})**
- **Provides click & pop suppression**
- **Improves PSRR**

- **The reference bypass capacitor plays an important role in the performance of the audio amplifier**
- **But…….**
  - *It adds to system cost*
  - *Takes up board space*
  - *Increases assembly time*

Too bad we can't get rid of the "But"…….

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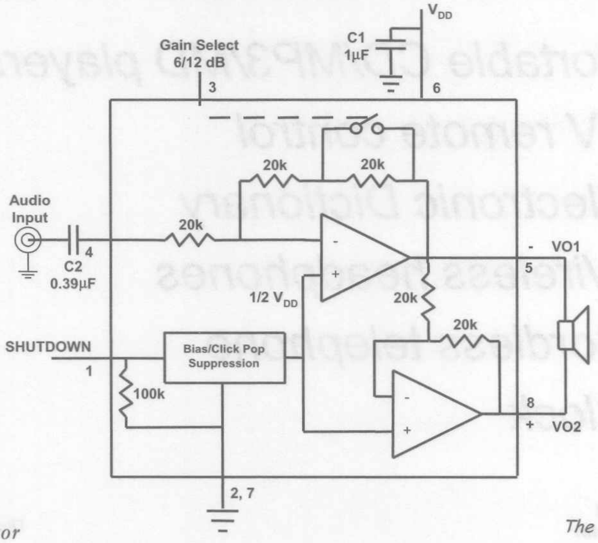
The Art of Analog 16

The reference bypass capacitor affects audio amplifier performance by the following ways:

1. Filters out noise on the input node. Along with an input resistor, the reference bypass capacitor forms a low-pass filter to minimize noise.
2. The size determines charging time to ½VDD (Wake Up Time, T_{WU}); the larger the capacitor the lower the slope at which charging occurs.
3. Click & Pop suppression is also determined by the size of the reference bypass capacitor; larger capacitances provide more resistance to sudden voltage changes.
4. The higher PSRR can be achieved with increasing capacitance but it comes at a cost of a longer wake up time.

Introducing the LM4906! Getting Rid of the "But"....... No Reference Bypass Capacitor Required!



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The Art of Analog 17

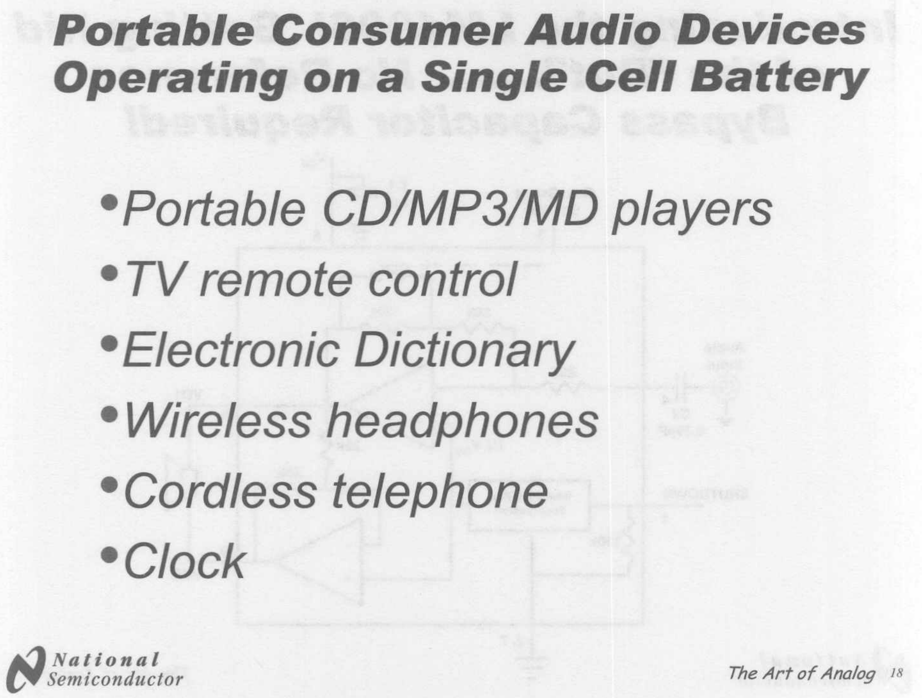
The LM4906 is the first Boomer® power amplifier that does not require an external reference bypass capacitor.
A new patented technology eliminates the need for the capacitor, resulting in a quick wake-up time (T_{WU}) , great PSRR specification, board space savings, and less assembly time.

The LM4906 requires only two capacitors (input capacitor and supply bypass capacitor), and has an internal gain (6dB or 12dB) setting pin.

Key Specifications:
V_{DD} = +3V
PSRR: 71dB @ 217 Hz; 73dB @ 1kHz
P_O = 390mW, R_L = 8Ω, BTL
T_{WU} = 4ms

V_{DD} = +5V
PSRR: 67dB @ 217 Hz; 70dB @ 1kHz
P_O = 1W, R_L = 8Ω, BTL
T_{WU} = 5ms

Applications:
Portable computers
Desktop computers
Multimedia monitors



Portable Consumer Audio Devices Operating on a Single Cell Battery

- Portable CD/MP3/MD players
- TV remote control
- Electronic Dictionary
- Wireless headphones
- Cordless telephone
- Clock

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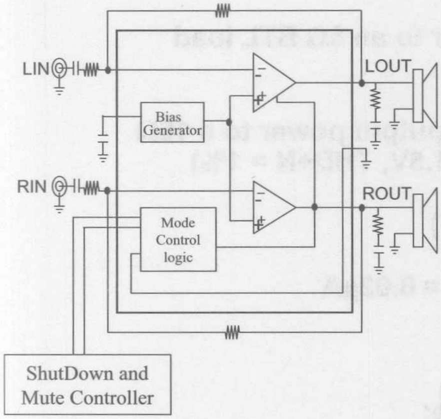
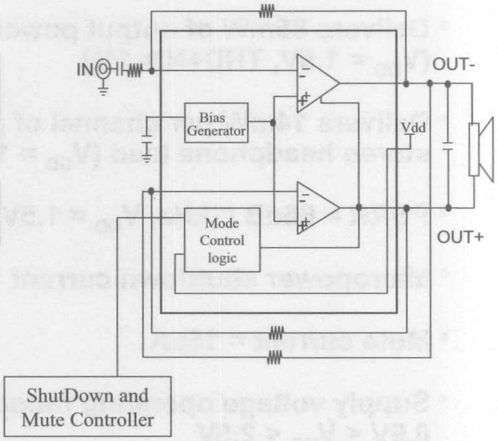
The Art of Analog 18

Most audio amplifiers suitable for portable devices operate between 3V to 6V. However, there are several portable consumer audio devices (as listed above) that only require a single cell battery, 1.5V, as the power source.

LM4916 Provides a Single-Cell Battery Solution





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The Art of Analog 19

The LM4916 is an audio power amplifier which operates on a 1.5V supply, therefore making it an ideal solution for portable, single-cell, audio products. The unity gain stable LM4916 features two modes of operation, a stereo headphone mode and a mono BTL speaker mode. It is capable of driving an 8W load in mono BTL mode and 16W in stereo headphone mode. The LM4916 also features a low current mute mode.

LM4916 – Mono 85mW BTL Output, 14mW Stereo Headphone Audio Amplifier

- **Delivers 85mW of output power to an 8Ω BTL load (V_{DD} = 1.5V, THD+N = 1%)**
- **Delivers 14mW per channel of putput power to a 16Ω stereo headphone load (V_{DD} = 1.5V, THD+N = 1%)**
- **PSRR = 66dB (1kHz, V_{DD} = 1.5V)**
- **Micropower shutdown current = 0.02μA**
- **Mute current = 15μA**
- **Supply voltage operating range: 0.9V < V_{DD} < 2.5V**

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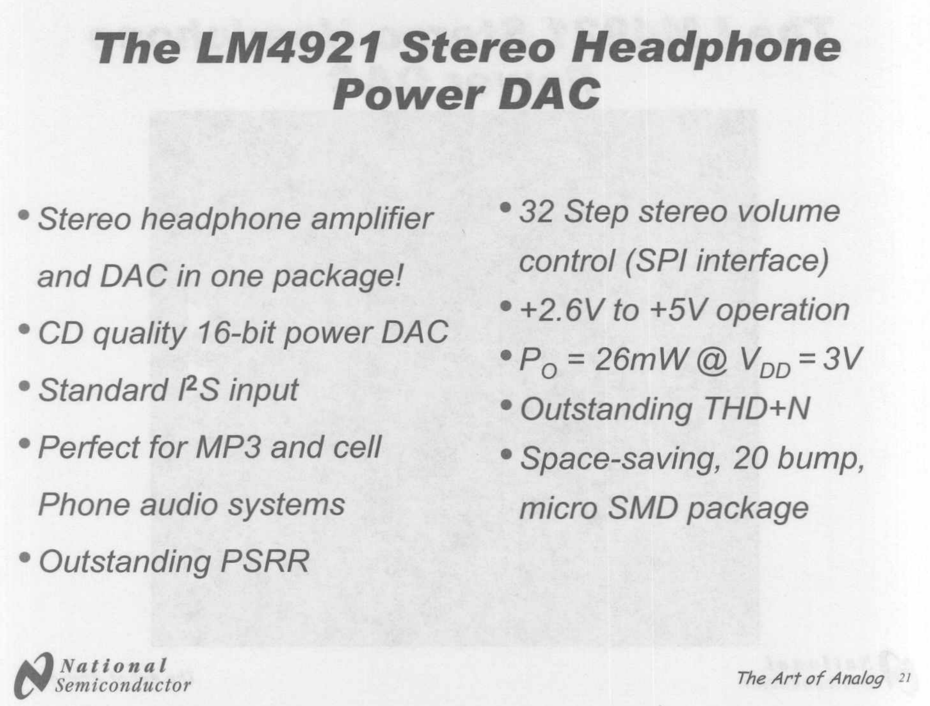
Operating on a single 1.5V supply, the mono BTL mode delivers 85mW into an 8 Ω load at 1% THD+N. In Single Ended stereo headphone mode, the amplifier delivers 14mW per channel into a 16Ω load at 1% THD+N. Additionally, the LM4916 features a low-power consumption shutdown mode, a low-current mute mode, "click and pop" suppression circuitry, and thermal shutdown.



The LM4921 Stereo Headphone Power DAC

- Stereo headphone amplifier and DAC in one package!
- CD quality 16-bit power DAC
- Standard I²S input
- Perfect for MP3 and cell Phone audio systems
- Outstanding PSRR
- 32 Step stereo volume control (SPI interface)
- +2.6V to +5V operation
- $P_O = 26mW$ @ $V_{DD} = 3V$
- Outstanding THD+N
- Space-saving, 20 bump, micro SMD package

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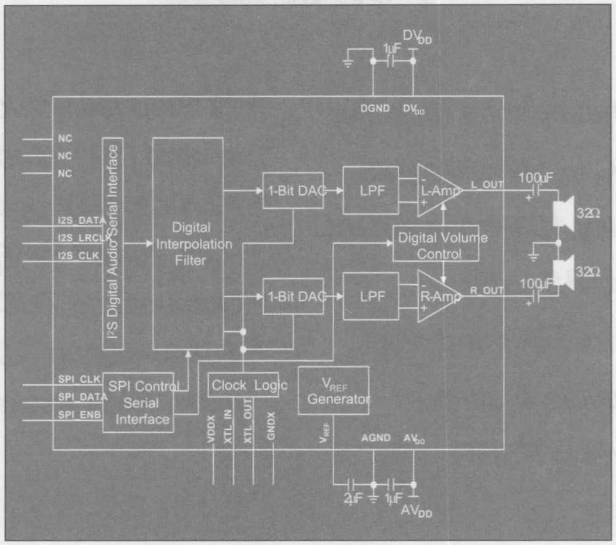
The Art of Analog 21

In today's demanding portable audio applications where features, size and cost are paramount, the LM4921 Power DAC is a perfect fit. In previous audio systems for portable handheld devices the DAC, Volume control and power amplifiers were in different packages which took up valuable space.. The new LM4921 combines a 16-bit resolution, stereo, I²S input, digital-to-analog converter (DAC) with a 1W per channel, stereo headphone, audio power amplifier. This new part saves both system design and board layout time while providing a simple to use, industry standard interface. National's industry proven 20 bump micro SMD package also saves valuable board space.

The LM4921's 16-bit/CD quality resolution provides a quality listening experience on a par with any portable devices in the market. The LM4921's superior 0.05% THD+N into a standard headphone load (32Ω) at 13mW makes the LM4921 suitable for any music or voice band applications.

The LM4921 Stereo Headphone Power DAC



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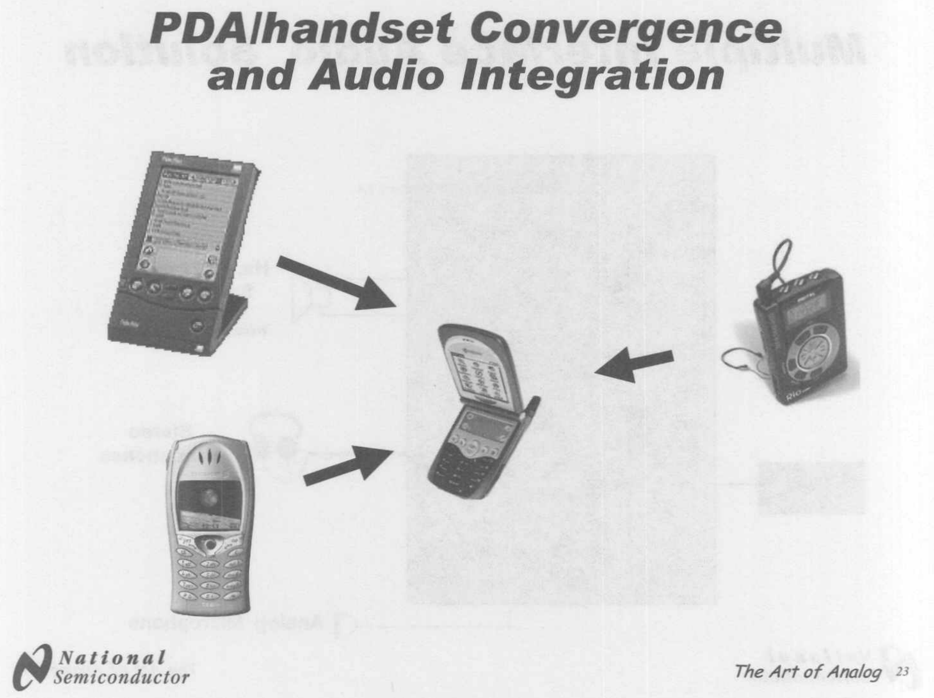
The Art of Analog 22

The LM4921 is primarily designed for demanding applications in mobile phones, PDAs and other portable communication device applications. The LM4921 features an I2S serial interface for the digital audio information and a 16-bit SPI serial interface for internal register control and communication. The LM4921 also features a programmable 32-step (1.5 dB per step) digital volume control accessed through the same easy-to-use SPI interface. The necessary clock signal can be externally generated or internally generated using an external crystal. It is, therefore, ideally suited for mobile phone and other low-voltage applications where minimal power consumption is a primary requirement. The LM4921 also features a low-power-consumption shutdown mode and an internal thermal shutdown protection mechanism.



PDA/handset Convergence and Audio Integration

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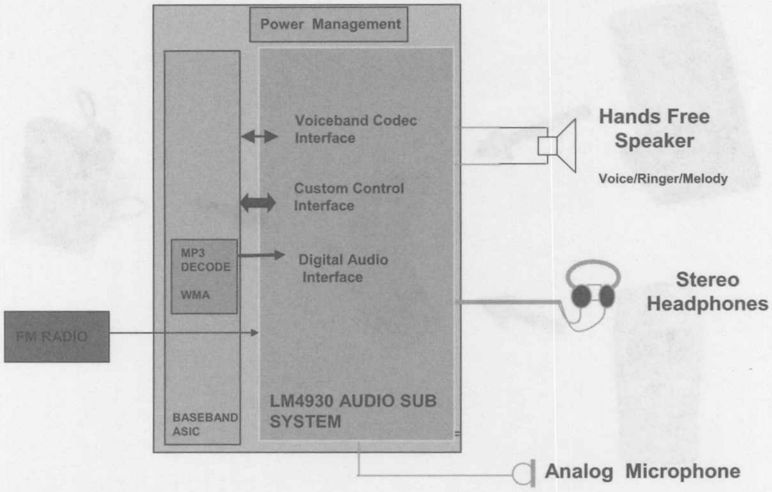
The Art of Analog 23

Today, the cellular handset is more than just a phone. It has quickly evolved into becoming a multimedia device, combined with the functionality of a phone, PDA organizer, and MP3/FM player. With all the increased features and demands required for today's handset, the audio amplifier solution for handsets has become increasingly complex.

Multiple Interface Audio Solution



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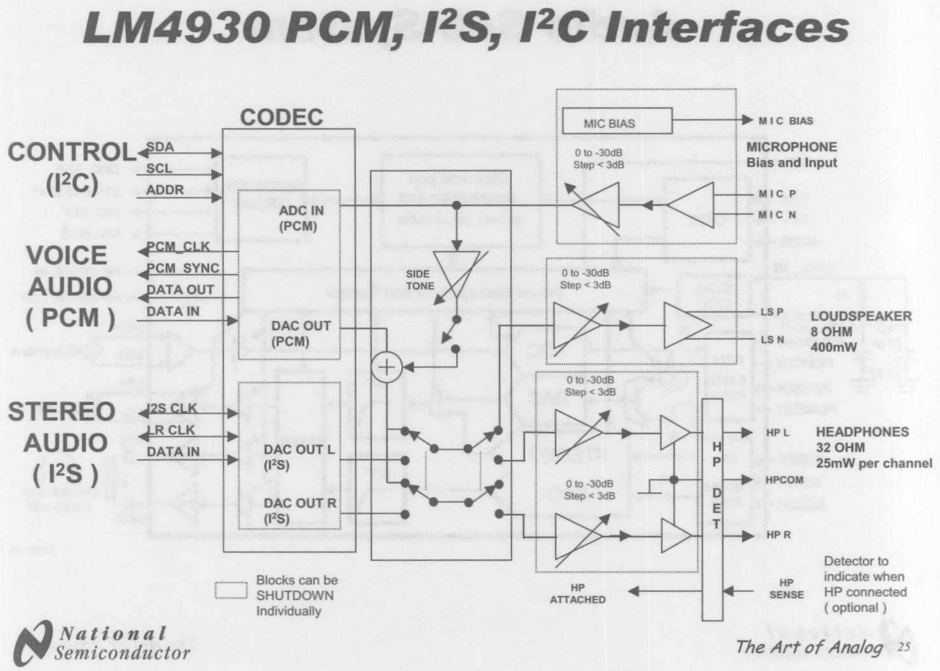
The Art of Analog 24

This diagram depicts the role of an audio subsystem in a cellular environment. The audio subsytem must be able to handle multiple audio interfaces, for voice data as well as high quality music from an MP3 decoder. Currently most solutions require a separate voice band codec and audio DAC to handle both voice and music data. The LM4930 integrates both the voice band codec and audio DAC, as well as the power amps required to drive both a hands-free speaker and stereo headphones into a single audio sub-system solution. An analog microphone input with ADC and full gain control of all inputs and outputs completes the system.

This system incorporates multiple audio modes where Voice or Audio may be sent to the mono output or the stereo headphone output, or even both at the same time! Full mixing and sidetone control are also integrated.



LM4930 PCM, I²S, I²C Interfaces

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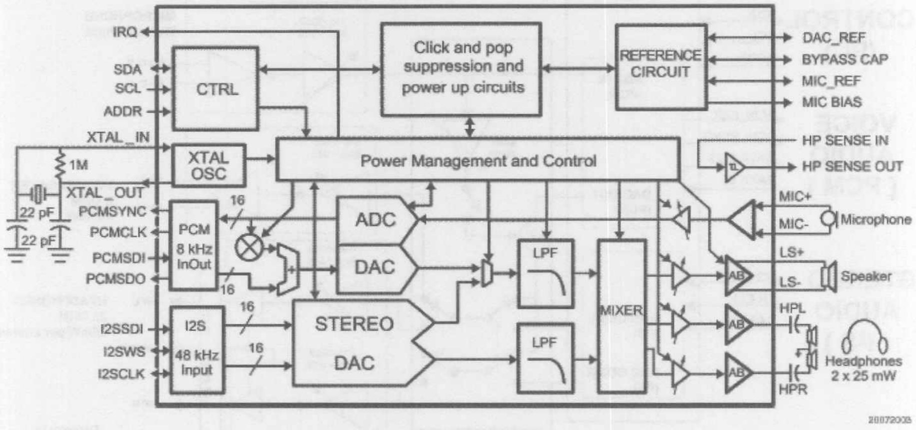
The LM4930's 48kHz DAC uses a standard I²S digital audio interface for stereo music playback. The integrated 8kHz voice band codec uses a standard PCM digital audio interface for voice data. The LM4930 also features an I²C compatible control (two-wire) interface to program both the voice band codec and audio DAC. For instance the LM4930 can be programmed to be either I²S master or slave mode. The PCM interface is master only. The I²C compatible interface can also program the LM4930 into different output modes as well as different volume control settings.

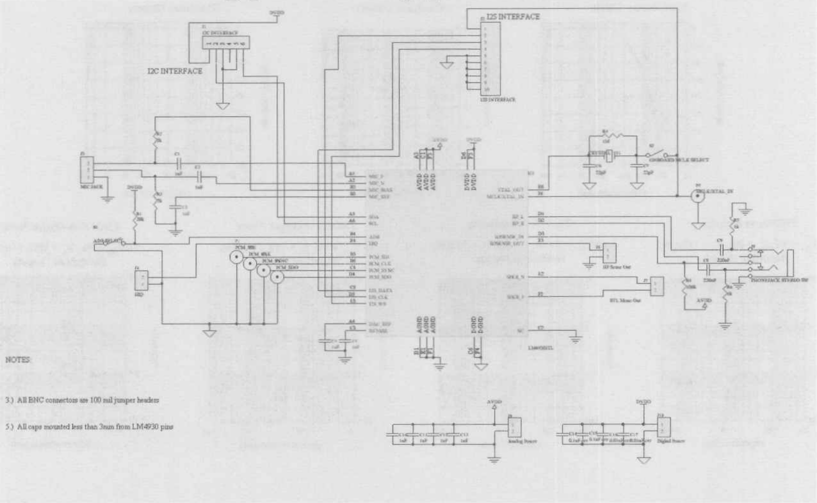
Audio Sub-System



Now integrated onto one IC:

- LM4930ITL, 36 bump micro SMD package
- All on same I^{2}C control bus
- Minimum amount of board space consumed (3.2mmx3.4mm)
- Reduced RF susceptibility system wide
- Enhanced power management and system-wide integrated click/pop reduction
- Minimum of external components
- Integrated filtering and mixing

LM4930 Audio Sub-System Typical Application



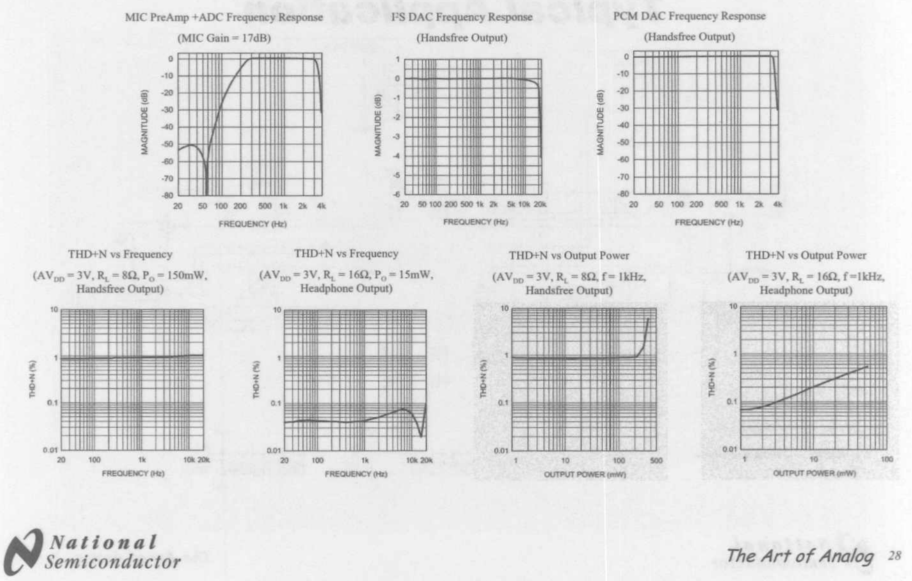
3.) All BNC connectors are 100 mil jumper headers

5.) All caps mounted less than 3mm from LM4930 pins

This shows the typical application circuit as given on the Reference Design Board. Note the small number of external components compared to separate system components. As an integrated system, the LM4930 enjoys many advantages vs. separate components: the single control bus reduces layout and system complexity, the small size and integrated traces reduces RF susceptibility system-wide, the integrated shutdown control reduces "click and pop" transients system-wide, low external component count, and best of all – small footprint (just 3.2mmx3.4mm in the 36-bump micro SMD package).

An external clock (Y1) option is shown in this diagram. The LM4930 is intended to be run off the 12.288MHz master clock of the baseband IC or micro controller.

LM4930 Performance



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The performance of the LM4930 is also in line with the rest of the boomer family. The top curves show frequency response for the MIC preamp +ADC stage, the I^{2}S DAC, and the PCM DAC. The frequency response for the MIC section is obviously affected by external cap values, but is near flat from 300-3kHz. The I^{2}S 16-bit DAC is near flat out to 20KHz – dropping only 0.4dB from 5kHz to 20kHz. The PCM DAC is also flat out to about 3kHz.

THD+N and Output Power for the internal BTL mono amp and single-ended stereo headphone amps are also excellent. THD+N is relatively flat for both the BTL out and the headphone out. The BTL output is capable of driving an 8 ohm load to 300mW with less than 2% THD+N. The headphone output has improved THD+N, with almost 50mW of power being delivered to a 16 ohm load at less than 0.5% THD+N.

History of Boomer® Amplifiers

- **Boomer amplifiers originally featured:**
  - *CMOS technology*
  - *BTL output(s)*
  - *5V supply operation*

From their inception, National's Boomer® audio amplifiers have taken advantage of a computer's available 5V power supply and rail-to-rail operation made possible by CMOS technology.

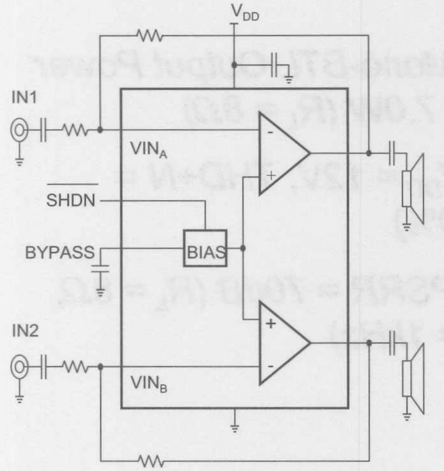
Modern Technology is Moving Away From 5V Supplies

- *Boomer® amplifiers now need to be powered by a 12V supply*

- *Want to retain superior performance of traditional Boomer amplifiers*

In many applications, a 1.8V digital supply is replacing the 5V supply, thus leaving a 12V analog supply to power audio circuitry. This creates a need for a new type of Boomer that maintains the superior performance of the previous generation of Boomers while powered by a 12V supply.

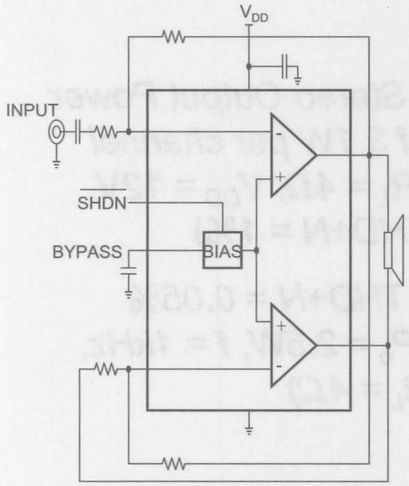
LM4950 – 7W Mono-BTL or 3.1W Stereo Audio Power Amplifier



- Stereo Output Power of 3.1W per channel ($R_L = 4\Omega$, $V_{DD} = 12V$, THD+N = 1%)
- THD+N = 0.05% ($P_o = 2.5W$, f = 1kHz, $R_L = 4\Omega$)

The LM4950 fills the need for a high performance audio amplifier that is also powered by a 12V supply. External resistors gives customers the option of setting the gain in either stereo SE or mono-BTL mode. In stereo mode, the LM4950 delivers an output power of 3.1W per channel (RL = 4Ω, THD+N=1%). It also has a THD+N of 0.05% at an output power of 2.5W (f = 1kHz, RL = 4Ω).

LM4950 – 7W Mono-BTL or 3.1W Stereo Audio Power Amplifier



- *Mono-BTL Output Power of 7.0W ($R_L = 8\Omega$)*
- *V_{DD} = 12V, THD+N = 10%)*
- *PSRR = 70dB ($R_L = 8\Omega$, f = 1kHz)*

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In mono-BTL mode, the LM4950 delivers an output power of 7.0W (RL = 8Ω, THD+N=10%) and has a PSRR of 70dB (RL = 8Ω, f = 1kHz).

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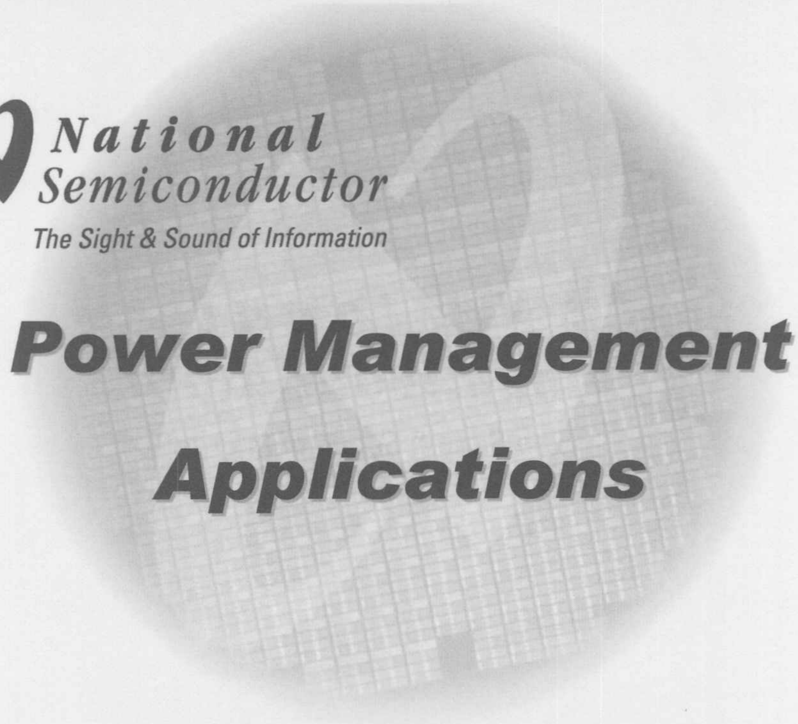
The Sight & Sound of Information



Power Management Applications

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The Sight & Sound of Information

Why use High Current Low-Dropout Linear Regulators?

↓

MINIMUM COMPONENT COUNT

↓

HIGH EFFICIENCY/LOW POWER LOSS

↓

NO EMI OR SHIELDING REQUIRED

↓

SMALLEST SIZE/LOWEST COST

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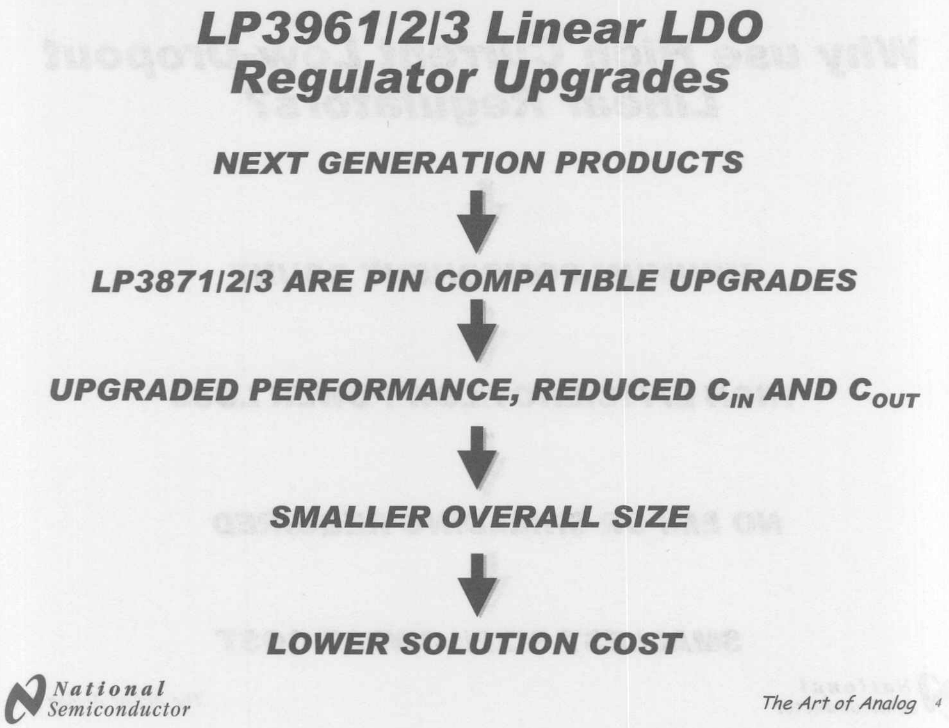
As electronic devices shrink in size and grow in circuit complexity, operating efficiency becomes critical. Traditionally, only switching converters offered high-efficiency in supplying regulated output voltages. These have the known disadvantages of higher component count, more complex design and layout, radiated EMI, and most important: higher cost.

Linear regulators which can operate with very low voltages across them are replacing switchers in many places. In today's products, a main power bus of 3.3V (+/- 5%) must often be down converted to lower voltages such as 2.5V. Instead of adding another output to the switcher, a low dropout (LDO) linear regulator can perform this function with low power dissipation.

In currents up to 3A, a 3.3 - 2.5V LDO design built around a device in a TO-263 or TO-220 package can deliver the full 3A utilizing only the PC board for heat dissipation, making this a compact and cost-effective design approach.



LP3961/2/3 Linear LDO Regulator Upgrades

NEXT GENERATION PRODUCTS

↓

LP3871/2/3 ARE PIN COMPATIBLE UPGRADES

↓

UPGRADED PERFORMANCE, REDUCED C_{IN} AND C_{OUT}

↓

SMALLER OVERALL SIZE

↓

LOWER SOLUTION COST

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The Art of Analog 4

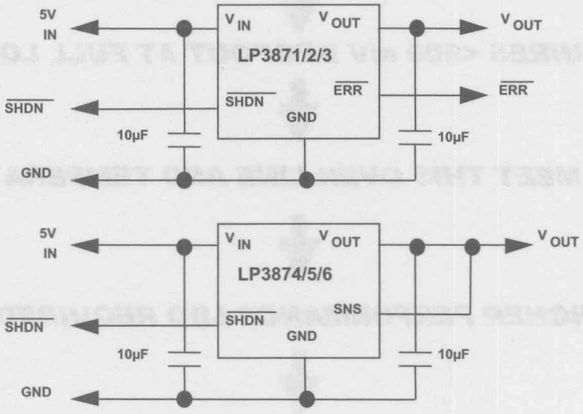
The LP396X product line of 0.8A, 1.5A, and 3A regulators has been widely used in applications such as switcher post-regulators, bus terminators, and general-purpose low-voltage requirements.

An unattractive feature of that family is that the external capacitors required for stability on the device are not trivial in size. To improve upon that, the LP387X product family was developed specifically to provide a drop-in replacement for the LP396X which requires only 10uF of CIN and COUT for stability.

Another improved parameter of the LP387X family is significantly higher AC ripple rejection, which means the parts more effectively reject noise on the input line.

The operation of the shutdown input of the LP387X is also improved: both the ON and OFF state voltages are ground referenced and can be driven from a logic gate. The LP396X "HIGH" voltage specification for the shutdown pin was referenced to the input voltage, which is not as simple to drive.

LP387x Pinout Options: Error Output or Remote Sense



ADJUSTABLE OUTPUT VERSIONS WILL ALSO BE OFFERED

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The Art of Analog 5

Pin 5 of the LP387X devices performs a different function depending on type. Each current version (0.8, 1.5, and 3A) is offered with that pin as either an ERROR output or remote sense function. Adjustable output voltage versions of the LP385X and LP387X products are planned for release in August 2003. For the adjustable versions, pin 5 will be the Adjust pin used to set the output voltage via external resistors.

3.3v (+/- 5%) to 2.5v Conversion

REQUIRES <600 mV DROPOUT AT FULL LOAD

MUST MEET THIS OVER LINE AND TEMPERATURE

HIGHER PERFORMANCE LDO REQUIRED

NSC LP3853/6 (3A) LDO's FOR THIS APPLICATION

The trend toward ever-reducing voltages means that low dropout regulators must continue to operate at lower voltage differentials. One key application is the task of regulating 3.3V (5%) down to 2.5V. The LP3853/6 was developed specifically to provide a 3A LDO solution which can meet this requirement. It is pin compatible with the existing LP396X and LP397X products.

Like the LP387X, it provides the same performance improvement over the LP396X of higher AC ripple rejection and simpler shutdown pin operation.

Adjustable output voltage versions of the LP385X and LP387X products are planned for release in August 2003.

Dropout Voltage Comparison

	LP396X	**LP387X**	**LP385X**
Max V_{DROP}@ 0.8A	350mV	350mV	N/A
Max V_{DROP}@ 1.5A	550mV	550mV	380mV
Max V_{DROP}@ 3A	1200mV	1200mV	600mV

Dropout voltage (defined as the minimum input-to-output voltage required to maintain regulation) is the key specification for all LDO regulators, as it determines how much power must be dissipated in the regulator. Compared to the LP396X and LP387X families, the LP395X products provide significantly lower guaranteed dropout voltage.

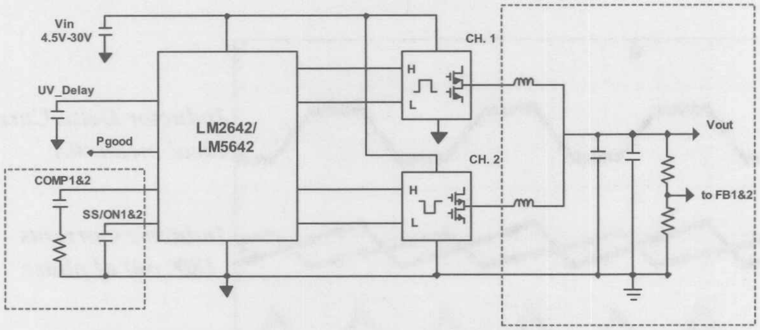
Ripple Rejection Comparison
(F = 120Hz)

CONDITIONS	***LP396X***	***LP387X***	***LP385X***
$V_{IN} = V_{OUT} + 1V$ $C_{OUT} = 10\mu F$		73dB	73dB
$V_{IN} = V_{OUT} + 1.5V$ $C_{OUT} = 100\mu F$	60dB		
$V_{IN} = V_{OUT} + 0.5V$ $C_{OUT} = 10\mu F$		57dB	57dB
$V_{IN} = V_{OUT} + 0.3V$ $C_{OUT} = 100\mu F$	40dB		

The PSRR (power supply ripple rejection) of a voltage regulator is a measure of its ability to reject the ripple on the input and not pass it through to the regulated output. Improving this parameter requires increasing the loop gain of the regulator at the frequencies to be eliminated.

One problem common to all regulators is that their loop gain typically starts to drop as the input voltage is reduced and the pass FET goes into its saturation region. The improved AC performance of the LP387X and LP385X devices are clear: Even with only a 10uF output capacitor (compared to 100uF for the LP396X), the LP387X and LP385X devices provide 13 dB more rejection with only 1V across the pass FET (compared to 1.5V for the LP396X). Similar improvement is also seen as the devices are pushed farther into saturation.

Operating a Buck Regulator in Dual-Phase Parallel Mode



Why use dual-phase?

The benefits of "current sharing" between two channels

- *Smaller inductors*
- *Lower output ripple*
- *Smaller input cap*
- *Better heat dissipation*

Using two buck regulators in parallel to provide twice the load current has several advantages over a single phase system.

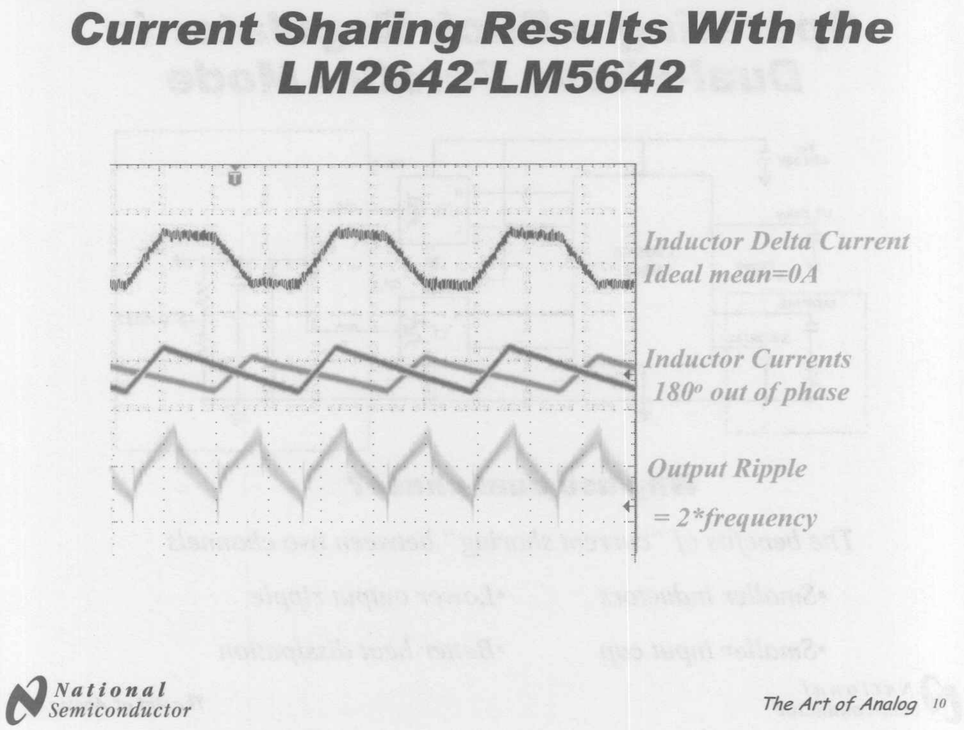
First, notice that the load current is shared by the two inductors. This reduces the required size of each inductor, thus allowing for better thermal dissipation and less stress on the components.

Two-phase operation also means that the ripple frequency seen at the output is effectively doubled, which reduces the ripple voltage. As a result, smaller output capacitors can be used to achieve the same result as a single-phase system.

Finally, because the input current is shared by both channels, the input ripple current is reduced, which results in lower rms current requirements for the input capacitor.

The dual-channel controllers LM2642 and LM5642 are uniquely designed to be operated in dual phase mode to provide high load currents over a wide range of operating conditions.

The block diagram above shows the basics of how to create a dual-phase system. Both channels share output capacitors, feedback and compensation networks, and must be operating 180 degrees out of phase.



Current Sharing Results With the LM2642-LM5642

Inductor Delta Current
Ideal mean=0A

Inductor Currents
180° out of phase

Output Ripple
*= 2*frequency*

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The Art of Analog 10

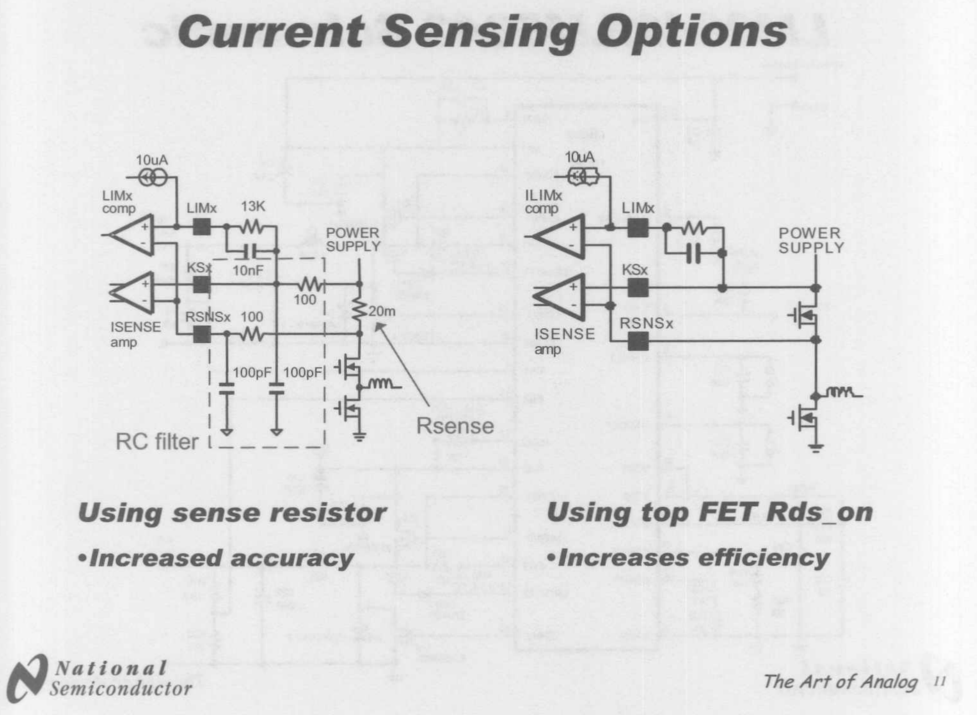
A dual-phase system requires good synchronization and accurate current sensing to ensure that both channels are sharing the load equally. As shown in the figure above, an ideal system will have equal and out-of-phase inductor currents.

Since the LM2642 and LM5642 were specifically designed for parallel mode operation, creating a dual-phase system is straightforward.

Each synchronous channel should be designed to handle half of the load current through the inductor. The output capacitors are designed for the full load current, but at twice the frequency. A single feedback network and a single compensation network is used for both channels. No synchronization is needed, since the two channels are operating out of phase on a single device. Because the two channels must start up simultaneously, the two enable pins are connected.

In this configuration the LM2642 and LM5642 can provide output currents above 10A with typically less than 500mA difference between the two parallel channels. This means that you can expect stable and reliable operation without having to over-design the individual power stages.

Because these devices are current-mode controllers, accurate current sensing is required to ensure equal current sharing. In dual-phase mode, current is Kelvin sensed via a sense resistor at the drain of the top FET of each channel.



Current Sensing Options

Using sense resistor

- **Increased accuracy**

Using top FET Rds_on

- **Increases efficiency**

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The Art of Analog 11

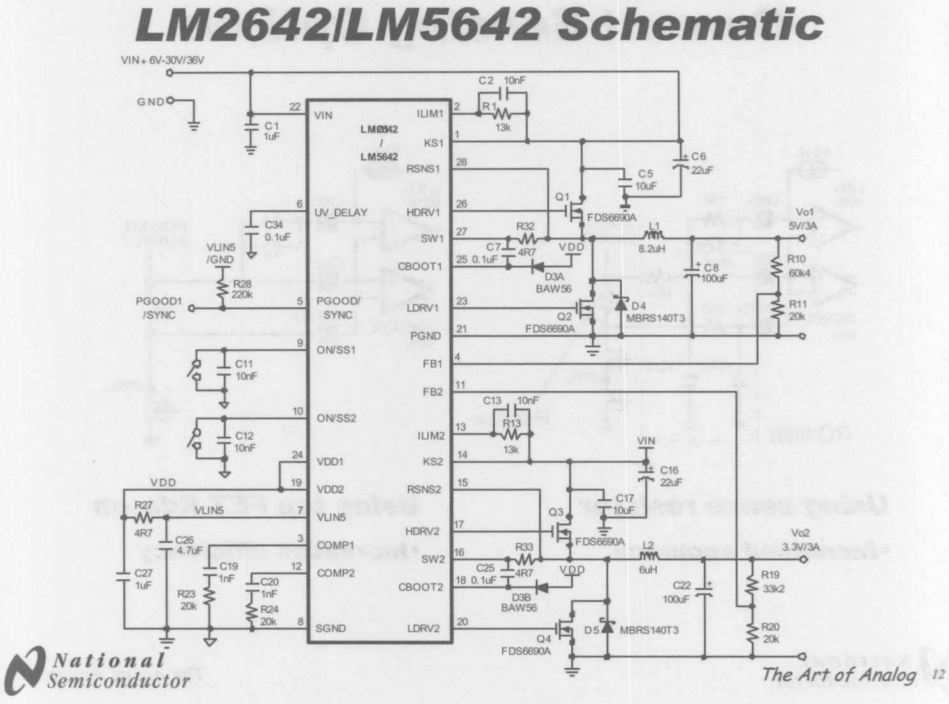
In a current mode architecture such as employed in the LM2642 and LM5642, there are two methods of sensing current, either across a current sensing resistor, or across the Rds_on of the top FET. There are advantages and drawbacks inherent to each method.

Using a sense resistor provides better accuracy because the value of Rsense will not vary with temperature and load current as much as the Rds_on of a FET. However, using a sense resistor by definition adds resistance to the current path, which will degrade efficiency.

Alternately, sensing current across the top FET is more efficient and reduces component count, but does not provide the accuracy of a sense resistor. For this reason, sense resistors are recommended when operating in dual-phase mode.

In the figure above at the left, note the two resistor capacitor pairs labeled “RC filter”. This illustrates another benefit of using a sense resistor. Isolating the current sensing nodes from the switch node with a sense resistor allows these RC filters to be installed.

These filters will further increase the accuracy of the sensing, and can be especially helpful in high current or low-duty-cycle applications where switching noise is high.



LM2642/LM5642 Schematic

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The Art of Analog 12

This schematic shows a typical 2-channel application for either the LM2642 or LM5642. This application will provide 3A on two separate channels with adjustable output voltages over the full range of input voltage.

Note the separate soft-start pins which provide both adjustable soft-start time and independent enable for each channel. These pins can be connected together for simultaneous startup.

The capacitor at Pin 6 is used to set the delay time for under-voltage latch off – UVP can be easily disabled by grounding this pin.

Pins 2 and 13 each connect to a single resistor which sets the cycle-by-cycle current limit for each channel. In this schematic, current is sensed across the top FETs and compared to a constant current across the current limit resistor.

Also notice the simple two-component compensation scheme, typical to current mode architecture, connected at COMP1 and COMP2.

Pin 5 is used for a power good flag on the LM2642 and a synchronization input on the LM5642. PGOOD is an open drain flag which goes low during a fault condition. The SYNC pin allows for adjustable operating frequency, or can be pulled low as shown for fixed-frequency operation.

LM2642/LM5642 Features and Differences

LM2642	*LM5642*
•300kHz	*•200kHz*
•PGOOD	***•SYNC***
•4.5-30V in	*•4.5-36V in*
•OVP	*•OVP*
•UVLO	*•UVLO*
•UVP with delay	*•UVP with delay*
•Cycle by cycle current limit	*•Cycle by cycle current limit*

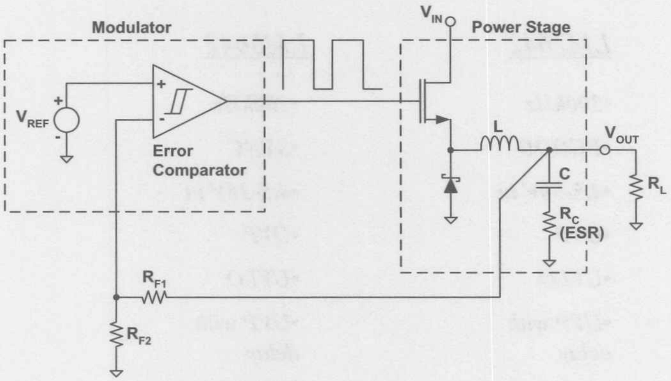
The flexibility and features of the LM2642 and LM5642 allow them to be used in a wide variety of high efficiency synchronous controller applications.

They have a similar set of features, including a wide input and output voltage range, over-voltage protection, input under-voltage lock out (UVLO), output under voltage protection with adjustable delay time, cycle-by-cycle current limit, and adjustable soft-start time.

There are a few important differences in features between the two devices, providing even more application flexibility. The LM2642 provides an open-drain PGOOD pin which goes low during any out-of-regulation or fault condition, and has a fixed operating frequency of 300 kHz. The input voltage range is 4.5V to 30V.

The LM5642 is designed for higher voltage applications with a maximum operating voltage of 36V. The LM5642 also provides a SYNC pin in place of PGOOD which allows the device to be synchronized to an external clock ranging from 150 kHz to 250 kHz. In general, synchronizing all the switching frequencies in multi-converter systems makes filtering of the switching noise easier. If SYNC is not used, the LM5642 operates at a fixed frequency of 200 kHz.

Hysteretic Architecture for Switching Regulators



Why use hysteretic control?

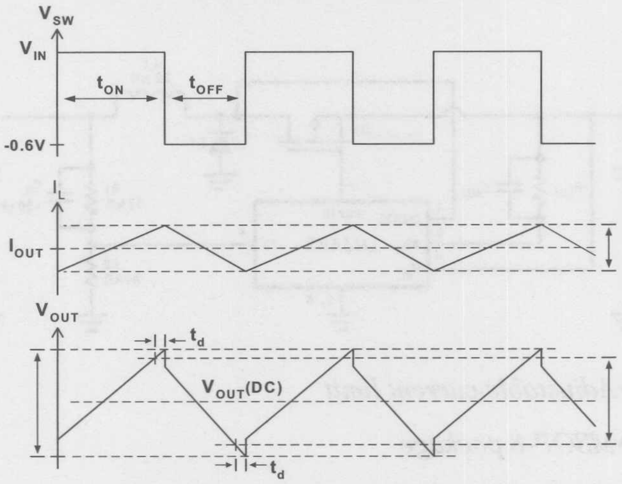
- Low component count
- No compensation
- Ceramic output cap.
- Excellent transient response

Hysteretic control is the simplest architecture available for a switcher. The modulator is simply a comparator with input hysteresis that compares the feedback voltage to a reference voltage. When the feedback voltage exceeds the reference hysteresis voltage, the comparator output goes low, turning off the switch. The switch will remain off until the feedback voltage falls below the reference hysteresis voltage, at which point, the comparator output goes high, turning on the switch and allowing the feedback voltage to rise again.

This simple topology provides several benefits. It is extremely fast at reacting to load and line transients. It has a very wide bandwidth control loop that doesn't use an error amplifier, and doesn't require frequency compensation. Thus, total component count is reduced, and output capacitance can be reduced.

Unlike a PWM regulator, switching frequency isn't set by an oscillator, but is dependent on several variables.

How it Works



$$f_{SW} = \frac{V_{OUT}}{V_{IN}} \bullet \frac{(V_{IN} - V_{OUT}) \bullet ESR}{V_{HYS} \bullet \frac{R_{F1} + R_{F2}}{R_{F2}} \bullet L \; + (V_{IN} \bullet ESR \bullet t_d)}$$

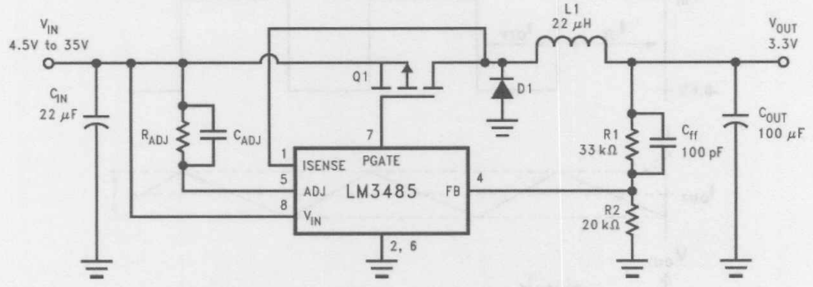
Hysteretic control is also known as ripple regulation, because it is the output ripple which controls the switching. The waveforms for a hysteretic buck regulator are shown above. The inductor ripple current generates an AC voltage across the output capacitor's ESR and ESL. This results in a triangle-shaped waveform at Vout. The output switch alternates on and off as the output waveform ramps beyond the upper and lower thresholds set by VHYS at the feedback node. Because of propagation delay, the peak to peak amplitude of the output ripple will extend slightly beyond these thresholds as shown above. Note that low ESL output capacitors must be used to keep the ripple step (seen in the Vout waveform) small and within the hysteretic window.

The equation above shows how switching frequency can be set using the external components. The output switch on time and off time (and therefore the frequency) are functions of the input and output voltage, the inductor, ESR and ESL of the output cap, the comparator's hysteresis, the feedback ratio, and the propagation delay (td) in the modulator and output stages. When designing a regulator, we can assume that VOUT, VHYS, the resistor feedback ratio, and td are constants. As a result, we select L and ESR for a desired frequency. However, frequency will vary with input voltage, so a range of operating frequencies should be selected, given a specified range of VIN.

Stable regulation is easy to achieve by making careful selections of the inductor and output capacitor ESR. In most cases, the output capacitor's ESR will dominate in determining both frequency and output ripple. Therefore, it is recommended that a low ESR ceramic output capacitor be used in series with a resistor to provide a stable ESR.

Output ripple can be determined by the following equation: Vrip=(Vin-Vout)*ton*ESR/L Where ton=duty cycle/frequency

LM3485 - PFET Hysteretic Control



- *Adjustable current limit*
- *MSOP-8 package*
- *PFET allows 100% duty cycle without bootstrap*
- *Cff speeds up operating frequency – up to 1MHz*

The LM3485 combines the simplicity of the hysteretic topology with high frequency operation (up to 1MHz) and an adjustable current limit. With a wide input and output voltage range of 4.5V-35V, the LM3485 offers great flexibility for use in a wide variety of applications.

Because this is a PFET controller, the switch is turned on by pulling the gate low. This means that there is no need for bootstrap circuitry to boost the gate drive voltage above the switch voltage. Therefore, the PFET can be kept on indefinitely, resulting in true 100% duty cycle operation.

Current limit can be adjusted with a single resistor R_{ADJ} which is connected to an internal current sink. The current limit operates by comparing the voltage across either the PFET or a sense resistor to the voltage across the current limit resistor. When the inductor current exceeds the current limit threshold, the PFET switch is turned off for a set period of time, effectively lowering the operating frequency.

A soft-start function can be created by placing a capacitor C_{ADJ} across the current limit resistor, as shown in the schematic above. This forces a lower current limit threshold during startup which limits the initial operating frequency and allows the output to ramp up more slowly.

A small capacitor (10pF-100pF range) can also be placed across the top feedback resistor as shown in the schematic above. This capacitor is used to increase the operating frequency in the following way:

The output ripple causes a current to be sourced or sunk through this capacitor. This current is essentially a square wave. Since the input to the feedback pin is a high impedance node, most of the current flows through the bottom feedback resistor, superimposing a square wave at the feedback node. The result is a reduction in output ripple and an increase in operating frequency. When using Cff, calculate the operating frequency using a value of 1 in place of the feedback resistor ratio.

LM2647
Synchronous Dual Channel Buck Controller

National
Semiconductor

This controller is intended primarily for mobile computing applications by virtue of its high efficiency (synchronous rectification) and its ability to produce sub-volt outputs over a wide input range extending from 5.5V to 28V. The range of output voltages possible is 0.6V to 5V (over the entire input operating range). Note that higher output voltages are 'allowed' if the application's input voltage range is smaller. The IC requires an additional low-power fixed 5V rail to provide power to the chip and to drive the two external N-channel FETS (per channel). N-channel FETs are cheaper than P-channel FETs, for a given value of Rds(on) and voltage rating.

LM2647 Features

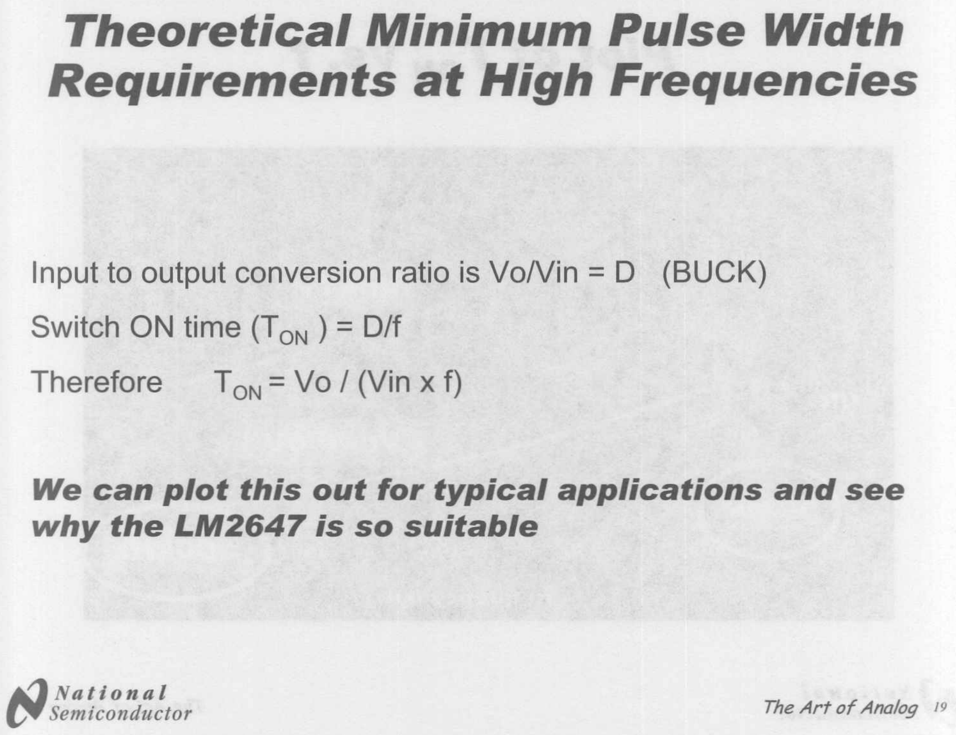
- Two independent channels: can be set from 0.6V to 5V over the input range 5.5V to 28V
- Interleaved switching for reduced input filtering requirements and size of capacitor
- Unusually narrow pulse widths possible
- Input feed-forward for fast line correction
- Adaptive Duty Cycle Clamp for long-term reliability

Interleaved switching refers to the fact that the two channels run 180 degrees out of phase. Since they don't draw current pulses at the same moment, the input current is effectively distributed over the switching cycle, resulting in lower peak and RMS input currents.

The capability to operate with extremely narrow pulse widths is an advantageous feature because it allows converting from a high voltage to a very low voltage without forcing the converter to go into a "pulse skipping" mode of operation.

Feed-forward compensation is a technique which effectively "bypasses" the error amplifier when responding to a change in duty cycle, resulting in faster output voltage correction when the input voltage changes abruptly.

The function of an adaptive duty-cycle clamp is to limit the duty cycle to a fixed percentage above the steady-state value, and yet not interfere with transient response. The limiting of the duty cycle prevents saturation of the inductor without requiring the size and expense of designing in additional "headroom" in the inductor's current capability.



Theoretical Minimum Pulse Width Requirements at High Frequencies

Input to output conversion ratio is Vo/Vin = D (BUCK)

Switch ON time (T_{ON}) = D/f

Therefore T_{ON} = Vo / (Vin x f)

We can plot this out for typical applications and see why the LM2647 is so suitable

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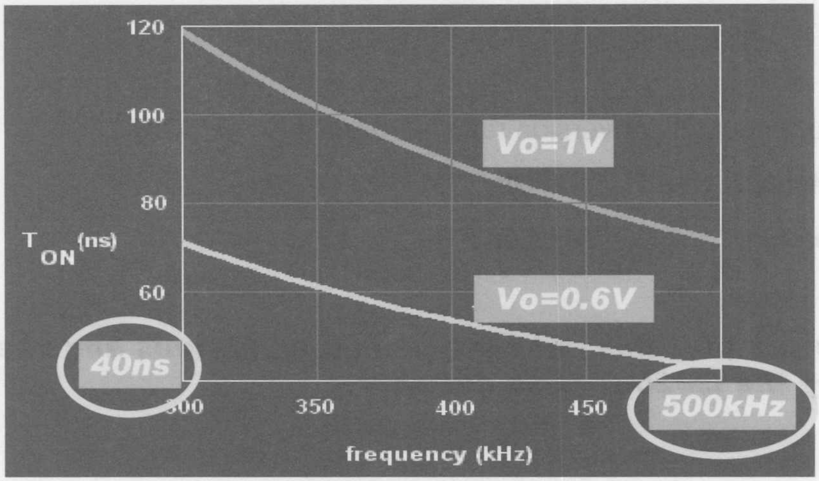
The Art of Analog 19

One of the main highlights of this IC is its ability to produce very narrow pulse widths. This makes conversion possible from a very high input to a very low output. Most other controllers cannot do this, and at high inputs, they usually respond by missing cycles in an effort to keep the output regulated, considering the fact that excessive energy was probably delivered in the previous pulse. This odd mode of operation results in high output voltage ripple and poor response to load transients. On the other hand the LM2647 assures proper functionality at extreme ranges. A look at the switching node waveform will reveal this fact.
Here it is demonstrated by a simple theoretical calculation above, and in the next slide.

Plot of T_{ON} vs. f



National Semiconductor

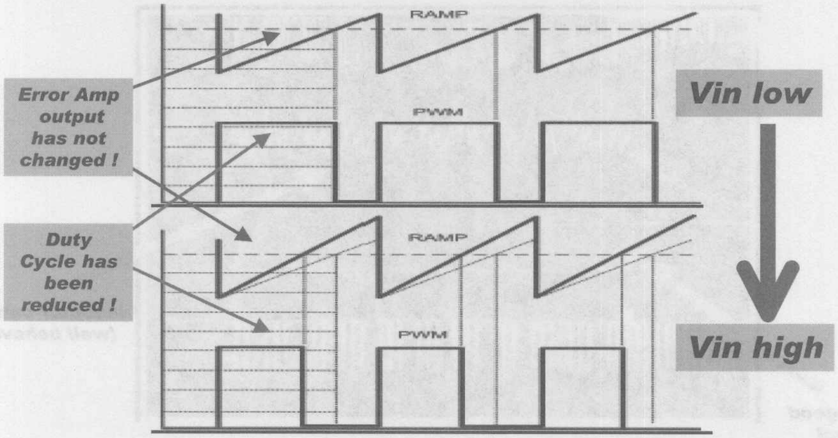
Note that Current Mode ('CM') controllers typically cannot achieve such narrow pulse widths. In CM control (since the sensed current forms the ramp to the PWM stage), the leading edge current spike can cause premature termination of the pulse. Therefore it becomes necessary to have a blanking time of about 100-200ns, during which time the controller basically turns a blind eye to the current, this translates into a minimum pulse width (of about 100-200ns).

From the above plot we can see that if we want to convert from 28V input to 1V output at 500 kHz, we need a pulse width of about 70 ns. But since each pulse of a typical CM controller is much larger than that, it will end up skipping cycles in an effort to maintain the output at its set value.

At an output of 0.6V from an input of 28V, the requirement is about 40ns at 500 kHz. This may be well beyond the capabilities of even most Voltage Mode ('VM') controllers (and well beyond the capability of CM controllers). The LM2647 can provide pulse widths of 30ns or less. This ensures the converter will operate without pulse-skipping.

The LM2647 is therefore a voltage mode controller which utilizes feed-forward. The input feed-forward used replicates the last remaining significant advantage of CM control within the framework of VM control.

What is Input Voltage Feed-Forward?



Error Amp output has not changed !

Duty Cycle has been reduced !

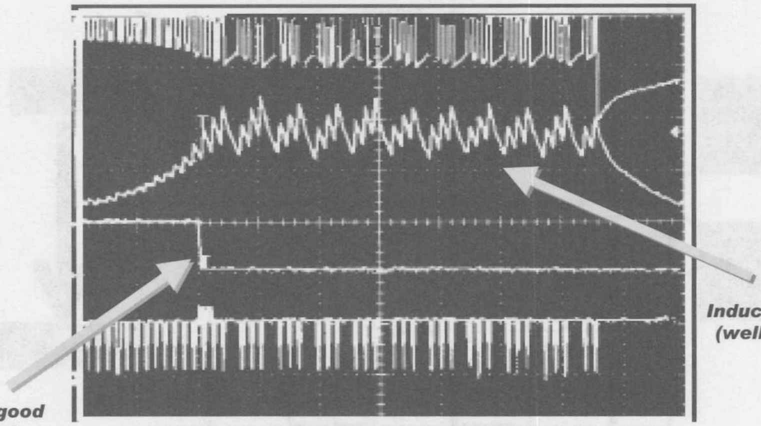
Vin low

Vin high

LM2647 simulates current mode control by changing slope of the PWM RAMP to mirror what the current ramp is doing. Duty cycle is immediately reduced without waiting for the error amplifier to respond, resulting in faster line transient correction.

Adaptive Duty Cycle Clamp

Behavior under severe overload or short circuit



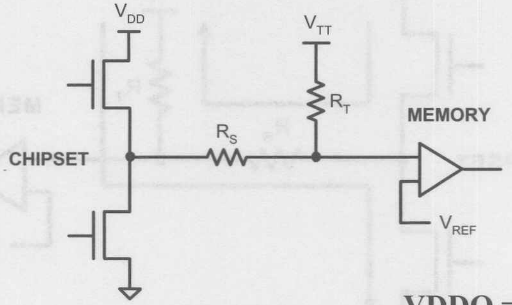
Inductor current (well behaved)

Power-good signal

The adaptive duty-cycle clamp is one of the unique features in the LM2647 which ensures excellent field reliability, and eliminates the need to oversize inductors or FETs. The LM2647 limits duty cycle to a calculated amount higher than the required steady-state value. This is very valuable in preventing huge current spikes (when the current sensing scheme is the low-side lossless type). The amount of duty cycle headroom provided in the LM2647 was carefully estimated at the design stage so as NOT to affect the transient response significantly even under severe step load changes.

SSTL-2 Active Termination

Termination scheme for DDR Memory



$$VDDQ = 2.5V$$

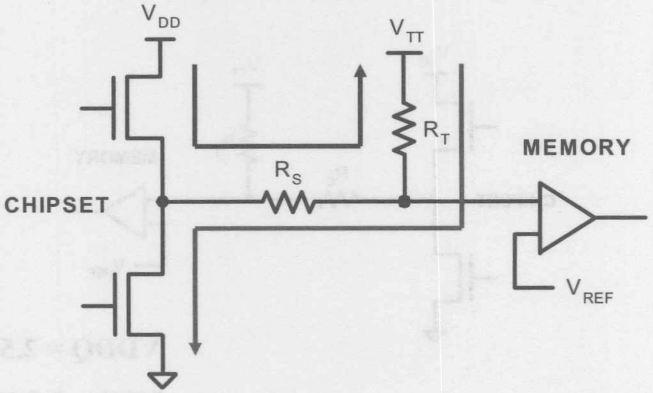
$$VTT = 0.5 * VDDQ$$

National Semiconductor

DDR (Double Data Rate) SDRAM memory poses a unique challenge over its predecessor SDRAM in that it requires active termination. The conventional termination scheme that is utilized is a single parallel implementation of the JEDEC SSTL-2 specification. This can be clearly seen in the drawing. The two resistors Rs and Rt are usually around 25 Ohms dependent on the impedance of the line, and are implemented on each of the address, data and command lines of the memory.

The memory core VDDQ requires a 2.5V rail that can be supplied by a buck switcher such as the LM2727, while the VREF (reference voltage) and VTT (the termination voltage) will track the VDDQ voltage by a factor of exactly 50%. Both are nominally equal to 1.25V. The tolerance on the Vref rail is that it can be within 40 mV of (VDDQ / 2) while the VTT voltage is allowed to track Vref to within 200 mV. This is to allow VTT to be positioned for better noise margins if necessary.

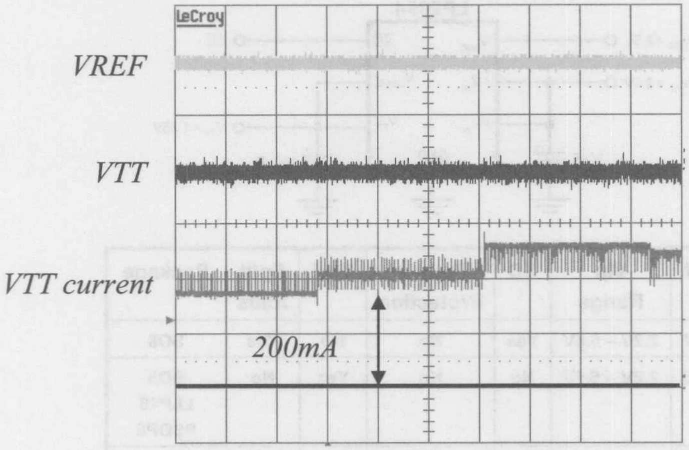
Calculating VTT output current



Unfortunately there are no definite specifications that exist on the amount of current that VTT is expected to supply. The first attempt to calculate the demands of the VTT power supply is to look at static conditions. If the chipset decides to write a “1” (high level) to the memory the output buffer shown will pull the Rs resistor to VDD, or 2.5V. This will cause a 1.25V drop across the series combination of Rs and Rt, since we know the memory is a high impedance. Therefore VTT will be required to sink 1.25V across 50 Ohms, or 25 mA. This can be seen by following the lower current path. The same analysis can also be applied if a “0” (low level) was written to memory. The same 1.25Volts would be seen across the resistors, except this time VTT would be required to source the 25 mA, shown by the upper current path.

If we used this 25 mA as a basis for the current requirements on each line, we would easily end up with a figure of over 3A for VTT in a typical memory configuration. This is assuming all the lines could be either high or low at the same time and remain in that state indefinitely. However, this is not a realistic expectation of the memory or power supply requirements. DDR is a dynamic memory that is switching at a clock speed of up to 200 MHz, and a data rate of 400 MHz. When we take into account the actual line impedances, and the cycles of memory, for instance, even with a typical read or write pattern the data lines are tri-stated the majority of the time; we can calculate the current requirements of VTT to be significantly lower.

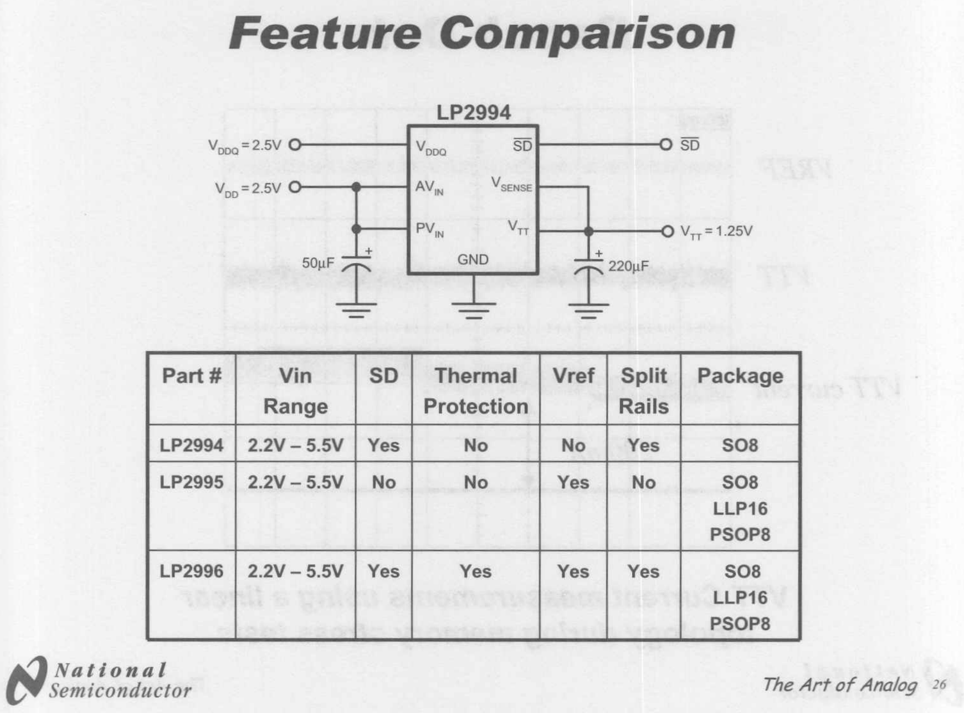
Bench Data



VTT Current measurements using a linear topology during memory stress tests

To confirm this we tested multiple systems and measured the VTT currents in a worse-case condition. What we found was that even under a worse case condition the VTT currents never exceeded 250 mA. This number now allows a linear solution to be utilized as opposed to a switching regulator to deliver 3A. The benefits of a linear topology are fairly clear: There is a lower component count and lower cost as inductors are no longer required. It's easier to use and simpler to design in. Also, there is increased performance since you do not have to worry about voltage ripple concerns.

If we look at an implementation of a linear solution during a stress test several features can be seen. The oscilloscope waveform depicts a PC memory system being tested with a memory stress test. The 3 patterns seen are reading all "0"s then writing all "1"s and reading all "1"s through memory. This has the effect of setting all the data lines in one state or the other. As can be seen, the average current is nominally around 200 mA with a worse case at 250 mA. During this entire time both VTT and VREF are extremely stable (both waveforms are AC coupled at 20mV per division)



Feature Comparison

LP2994
V_{DDQ} = 2.5V
V_{DD} = 2.5V
V_{DDQ}
AV_{IN}
PV_{IN}
$\overline{SD}$
V_{SENSE}
V_{TT}
GND
$\overline{SD}$
V_{TT} = 1.25V
50µF
220µF

Part #	Vin Range	SD	Thermal Protection	Vref	Split Rails	Package
LP2994	2.2V – 5.5V	Yes	No	No	Yes	SO8
LP2995	2.2V – 5.5V	No	No	Yes	No	SO8 LLP16 PSOP8
LP2996	2.2V – 5.5V	Yes	Yes	Yes	Yes	SO8 LLP16 PSOP8

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The Art of Analog 26

To provide a linear solution to address DDR memory termination, National Semiconductor has released three products, the LP2994, LP2995 and LP2996. Each one is capable of terminating the memory with differences in feature sets to suit your application needs. Some key features on the parts are that they internally generate the divide by two voltage for tracking VDDQ without the need for external resistors. The LP2995 and LP2996 both provide a VREF output for the chipset and memory, while the LP2994 and LP2996 contain a shutdown pin that will tri-state VTT to allow a suspend-to-ram (STR) state to be achieved. These two parts also have the ability to split the power and bias rails which allows the internal power dissipation to be lowered. All of these parts are released and can be found on the website.

Why Boost Converters?

LOW VOLTAGE POWER RAILS

↓

HIGH VOLTAGE REQUIREMENTS

↓

**DEDICATED HIGH -EFFICIENCY
BOOST CONVERTERS**

The trend in all electronic systems is toward utilizing lower main power supply voltages in order to reduce power consumption and increase operating efficiency. However, some circuitry requires higher voltage rails to operate. In many cases, the only cost-effective solution is to use high-efficiency boost converters to generate a local rail that powers the higher voltage hardware.

KEY REQUIREMENTS FOR BOOST CONVERTERS

HIGH POWER CONVERSION EFFICIENCY

↓

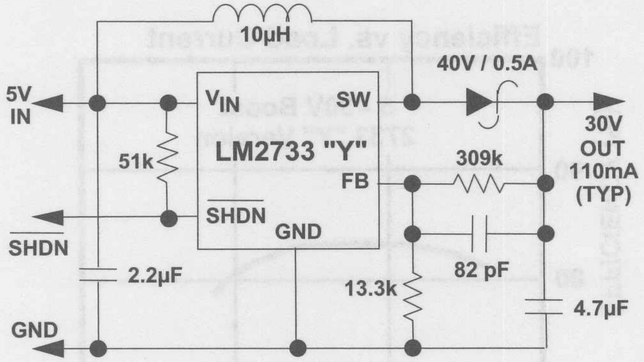
MINIMUM BOARD SIZE FOR TOTAL DESIGN

↓

LOW COST

Boost converters have to have high-efficiency if they are to achieve small size, since internal power dissipation has to be kept to an absolute minimum. The cost-driven nature and size restrictions of these applications means that small external components (inductors and capacitors) must be used. This forces the operating frequency of the converter to be very high, which typically makes it more difficult to maintain high-efficiency because switching losses start to become the predominant power loss factor. The key design challenge is to make an IC boost converter that has small package size and yet has an internal switch that can handle high peak currents with low ON resistance and minimal switching losses.

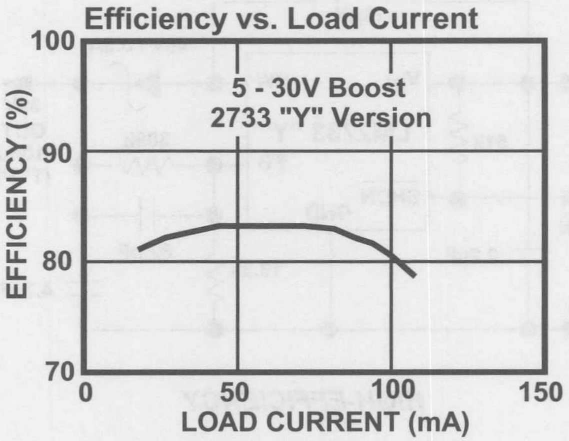
5 – 30V Boost Converter



HIGH-EFFICIENCY
SMALL COMPONENT SIZE

The LM2733 is a high-frequency boost converter in the SOT-23 package with a built-in FET switch rated at 40V and 1A current. It is targeted for applications requiring output voltages above 20V (for under 20V, see the LM2731).
The application shown is a typical usage where a 5V rail is used as the primary power. The "X" version of the device operates at 0.6 MHz, while the "Y" version operates at 1.6 MHz. As shown, the LM2733Y is capable of delivering more than 3W of load power when powered from a 5V supply. Small ceramic capacitors are used for both input and output, reducing cost and size. Because of the high operating frequencies, small inductors can be used and still deliver maximum load power.

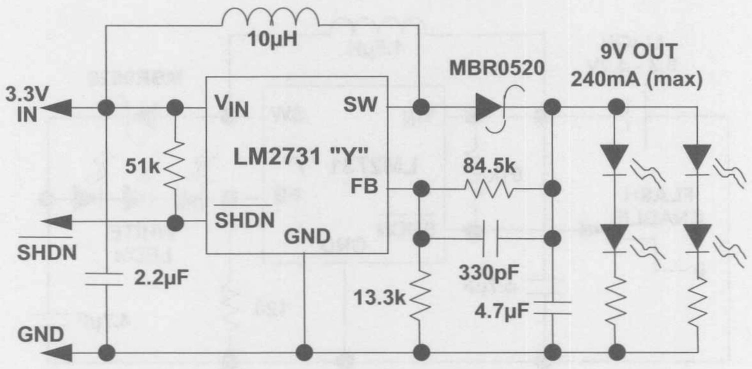
5 - 30V BOOST EFFICIENCY



Efficiency is the key design parameter in most cases, as it limits maximum ambient operating temperature and in many cases, how much load power can be delivered.

As shown, this particular application maintains efficiency between 80 and 85% for most of the usable operating current range. This means that even at full load current, the internal power dissipated in the entire converter is less than about 0.6W that is, distributed between the inductor, rectifier diode and internal FET switch of the LM2733. This high-efficiency means that this design could safely operate in ambient temperatures as high as 50°C.

3.3V - 9V LED BACKLIGHT SUPPLY



LED's DRIVEN AS A CONSTANT VOLTAGE LOAD

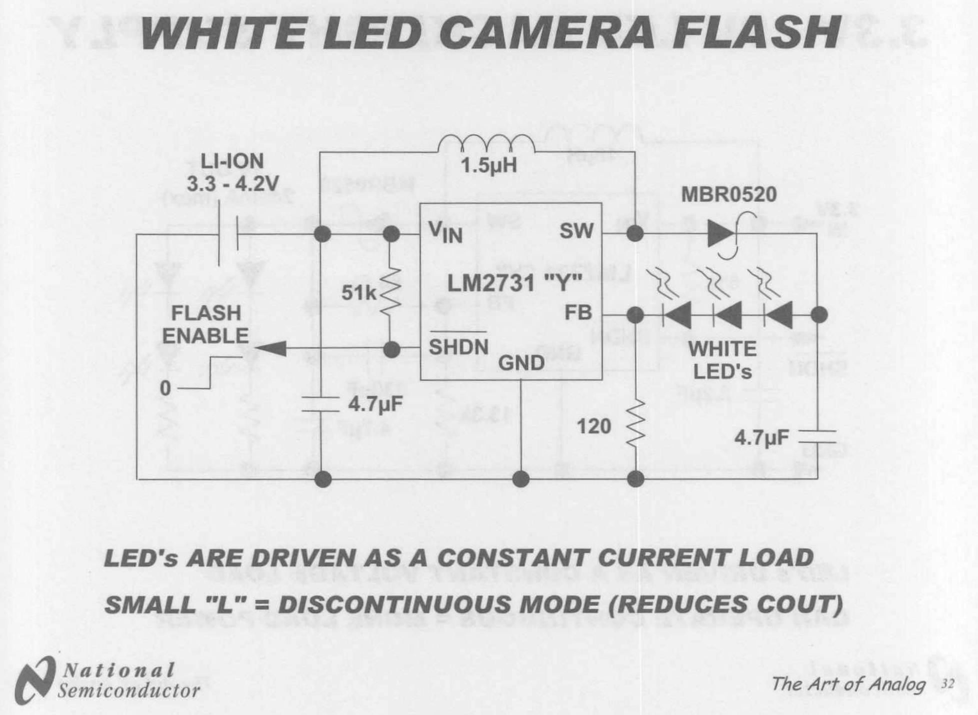
CAN OPERATE CONTINUOUS = MORE LOAD POWER

National Semiconductor

LED's are frequently used in portable applications for illumination because of their high brightness and efficiency. In this application, four LED's are connected in a series/parallel load configuration. Series resistors are used to set the current through the LED's. This design is built using the LM2731, which has a higher-current FET switch than the LM2733. It is optimized for applications where more current is needed and the output voltage is under about 20V.

The advantage of this particular load connection is that the LED's are driven from the output of the converter in the typical constant voltage mode of regulation. The regulator can operate in a continuous mode of conduction (where the inductor current never drops to zero) and still be stabilized with a small output capacitor. Continuous mode operation delivers maximum load power for a given input voltage. The primary disadvantage of this circuit is that the LED's are not driven by constant current, LED current will vary with LED temperature because their VBE voltages will change.

The next application shows how LED's can be driven as a constant-current load.



WHITE LED CAMERA FLASH

LED's ARE DRIVEN AS A CONSTANT CURRENT LOAD

SMALL "L" = DISCONTINUOUS MODE (REDUCES COUT)

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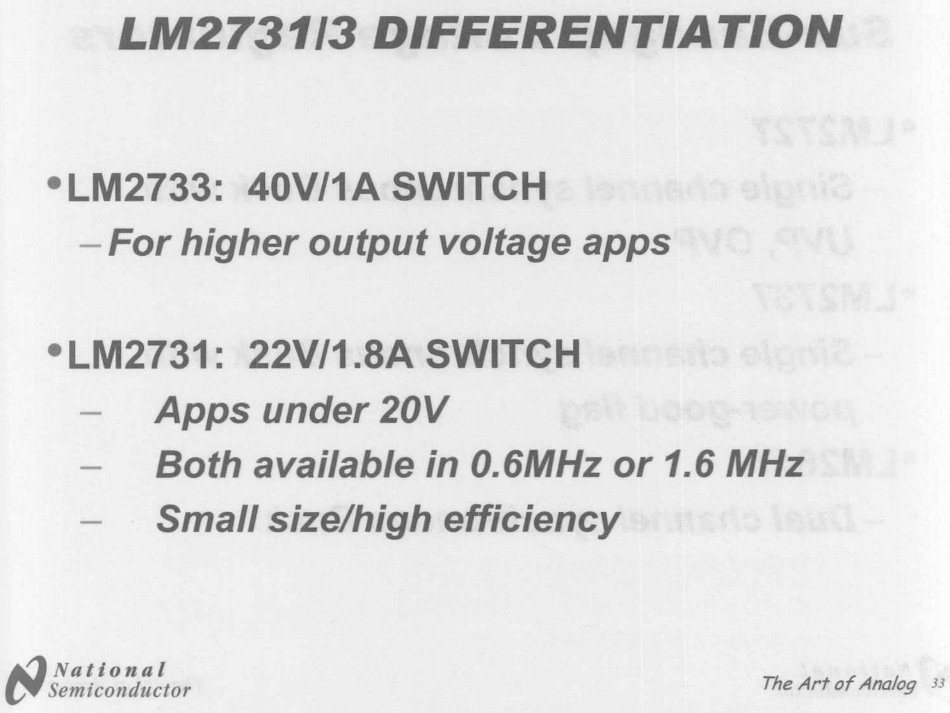
The Art of Analog 32

One of the most common applications utilizing the LM2731 is the white LED flash used in portable cameras. The important difference of this application is that the LED's are connected from the output to the feedback node. In operation, that will force a regulated current to flow through them whose value is the reference voltage divided by 120 (which would be about 10 mA for this case).

The effect of putting the LED's in place of the top feedback resistor is that for small signal analysis, the gain going from the output to the FB node is essentially unity. This means that larger output capacitors and/or smaller values of inductance are required for stable operation. For this particular application, the load current requirement is easily met using a 1.5 µH inductor which reduces both the size and cost of the inductor as well as reducing the amount of output capacitance required for stability. Using smaller inductors will allow the converter to operate in discontinuous mode where inductor current drops to zero on each switch cycle, which is actually a more stable mode of operation.

As a rule of thumb, a maximum inductance value of about 4.7 µH is the practical upper limit for this circuit and would probably require about 22 µF of output capacitance for stability up to maximum load current.



LM2731/3 DIFFERENTIATION

- **LM2733: 40V/1A SWITCH**
  - *For higher output voltage apps*
- **LM2731: 22V/1.8A SWITCH**
  - *Apps under 20V*
  - *Both available in 0.6MHz or 1.6 MHz*
  - *Small size/high efficiency*

National Semiconductor

The Art of Analog 33

The boost switcher products are divided into a higher-current, lower-voltage version (LM2731) and a higher voltage, lower current version (LM2733). This allows better utilization of the available die area within the SOT-23 package to minimize FET on resistance (and maximize efficiency) for different applications.

Both products are offered in both operating frequencies of 0.6 MHz and 1.6 MHz to allow the use of smaller inductor and capacitor values in applications where the higher frequency is feasible.

Sub-Bandgap Voltage Regulators

- LM2727
  - *Single channel synchronous Buck with UVP, OVP*
- LM2737
  - *Single channel synchronous Buck with power-good flag*
- LM2647
  - *Dual channel synchronous Buck*

National currently has three buck regulator controller products available that can provide output voltages below the traditional bandgap voltage, which is typically 1.23V.

LM2727 and LM2737:

-Controllers with external N-FETs: output currents up to 25A
-Adjustable switching frequency from 50kHz to 2MHz
-External compensation, voltage-mode PWM
-Can operate from 3.3V input
-Wide range of applications

LM2647:

-N-FET controller like the LM2727 and LM2737
-Dual channel with channels 180° out of phase: uses smaller input capacitors
-Voltage mode control designed to provide two different output voltages
-Adjustable switching frequency from 200 kHz to 500 kHz
-Takes input voltages between 5.5 and 28V
-Uses feedforward for faster transient response
-Vout as low as 0.6V with 1.5% tolerance
-PWM or pulse-skip modes
-Has output UVP and OVP, input UVLO, power-good, enable, soft-start

Uses for Sub-Bandgap Voltages

- Non PC CPUs (set-top boxes, gaming units)
- New DSP core voltage
- New ASIC voltage
- 1.2V Rail at 1.5% tolerance

The trend in voltage rails for almost all applications is towards lower voltages at higher currents. The main driving force behind this is CPU core power supplies, where voltages less than 1.0V can require currents higher than 30A. This is especially true for the emerging generation of portable computers which use lower voltage to increase efficiency and extend battery life. As CPUs lead the way, the core logic supplies for GPUs (graphics processing units), DSPs, ASICs, and other equipment follow. Newer products have tighter tolerances on their voltage rails, meaning that a voltage regulator with a minimum output of 1.23V can no longer be used to supply a 1.2V rail.

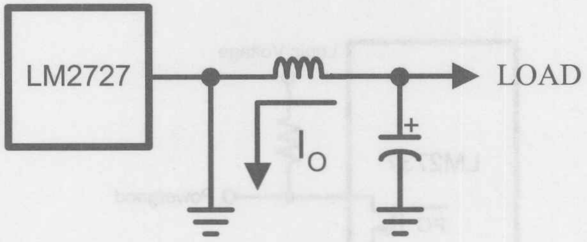
LM2727

- Synchronous Buck Regulator Controller
  - *Controls external N-FETs*
- Vout as low as 0.6V, Vin from 2.2 to 16V
- Adjustable switching frequency
- Has soft-start, OVP, UVP, UVLO, current-limit, thermal shutdown

The LM2727 was our first buck controller to feature a 1.5% tolerance reference voltage of 0.6V over the temperature range of 0 to 125°C. The wide range of input voltage (2.2 to 16V) allows buck conversion of voltages below 3.3V. Output voltage ranges from 0.6V up to approximately 90% of Vin when the converter is switching at 300 kHz or less. By driving external N-FETs, designs capable of delivering as much as 25Amps are possible. An adjustable switching frequency that extends from 50 kHz to 2 MHz allows optimization of inductor size and capacitor requirements for a specific application.

LM2727 CPU Geneology

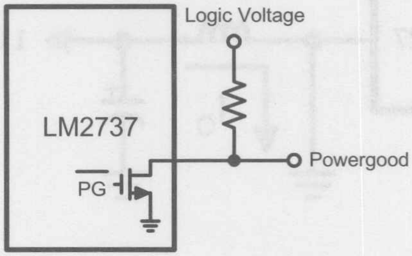
- Low side FET ON
  - *This feature is attractive to CPUs*



The LM2727 was developed from the LM2636, a product designed to meet the requirements of Pentium II™ CPUs. Although the LM2727 uses a pair of feedback resistors to determine the output voltage, it retains two features of regulators that are specific to CPU power supplies. First, the IC turns the low side FET on during faults. This discharges the output capacitors and protects the load. Second, the IC will latch off if the under-voltage protection (UVP) or over voltage protection (OVP) detect an ouput voltage that has dropped to below 70% of nominal or exceed 118% of nominal, respectively. Switching will not begin again until the Vcc voltage has been cycled or the EN pin has been cycled.

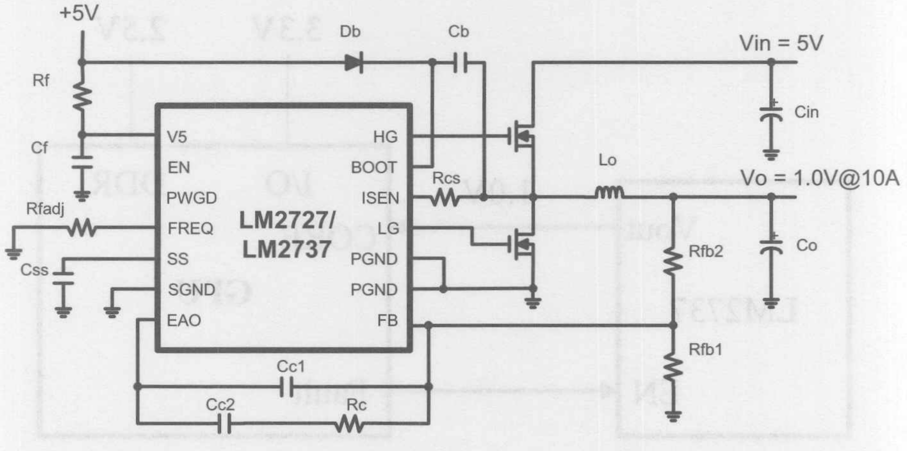
LM2737

- Pin-for-pin compatible with the LM2727
- No UVP or OVP
- Powergood flag can signal other circuitry



The LM2737 is not disabled during UVP or OVP conditions. It will continue to switch as long as the EN pin is open or connected to a logic high, voltage is available at the Vcc pin, and voltage is available at the drain of the top N-MOSFET. The internal comparators that disable the LM2727 signal an open-drain power-good pin instead. The circuit designer is free to use almost any voltage source with a pull-up resistor to signal other circuitry in the case of a fault.

Typical Application



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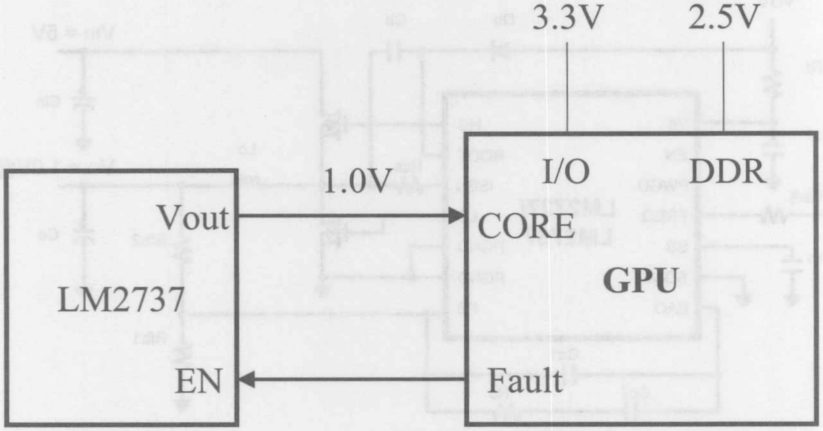
The possibilities for circuits are as varied as the selection of N-FETs, inductors, and capacitors that are available. For low currents, dual FETs in SUPERSOT-6 or SO-8, off-the shelf inductors, and ceramic capacitors can be combined with high switching frequencies. For higher currents, multiple FETs can be paralleled on top and bottom. Using large FETs with high power (and low cost) toroid inductors combined with lower switching frequencies delivers better efficiency. The LM2727 and LM2737 use a true internal op-amp combined with external compensation to ensure loop stability with a variety of output capacitors. Good phase margin and high bandwidth are possible with all types of caps, from aluminum electrolytics and tantalums to POSCAPS and "all ceramic" solutions.

GPU Power Application



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In this example, a graphics processing unit uses standard voltages of 3.3V and 2.5V for I/O, to run DDR memory and for logic signaling to and from other circuits.

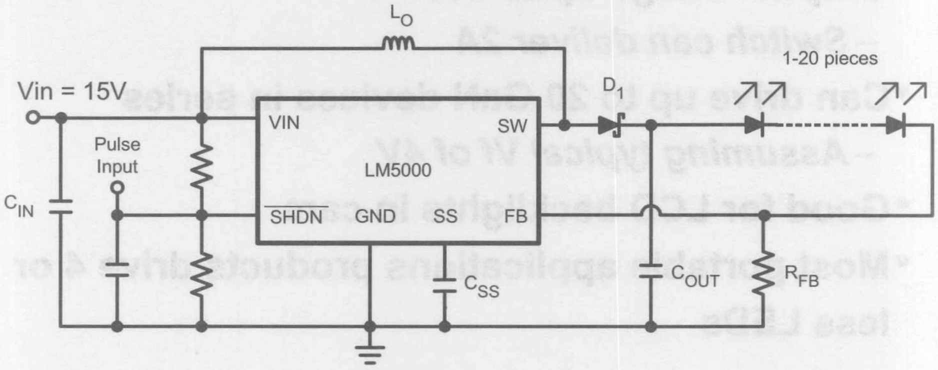
Even in a desktop PC, where battery life is not a constraint, low voltage is needed at the core of the device for increased operating speed and reduced heat (lower rail voltage = lower power dissipation.) Instead of a GPU, the load could be an ASIC controlling a hard drive, the processor in a gaming machine, etc.

LM5000 as White LED Driver

- Output voltage up to 80V.
  - *Switch can deliver 2A*
- Can drive up to 20 GaN devices in series
  - *Assuming typical Vf of 4V*
- Good for LCD backlights in cars
- Most portable applications products drive 4 or less LEDs

National has a variety of devices available which are designed to drive GaN (white, blue) LEDs. Even though the human eye can usually tolerate approximately 15% differences in brightness, it is sensitive to changes in color. GaN LEDs require constant current to maintain even coloration over large backlit areas. The existing devices ensure current matching by using a separate regulated current source (parallel designs, LM2794, LM2795) or by putting all the LEDs in series. (LM2703, LM2704) The constraint in these portable-targeted ICs is that they are designed to drive four or less LEDs each. Driving larger strings would require many more pins for parallel designs, and requires ever-higher voltage in series designs. The LM5000 can be used to create a much higher voltage boost converter. The application presented next shows the LM5000 used as the backlight driver for an automobile LCD display that uses 16 white LEDs with a forward current of 15 mA.

White LED Backlight Application



The LM5000 can accept input voltages ranging from 3.1 to 40V. In this circuit a nominal input voltage of 15V represents an unloaded automotive battery. Precise control over the current in the LED string is maintained by replacing the top feedback resistor with the LEDs themselves. (The same procedure used in lower-voltage constant-current LED drives.) Rfb is set so that the regulator increases the current passing through it until the feedback voltage Vfb is reached.

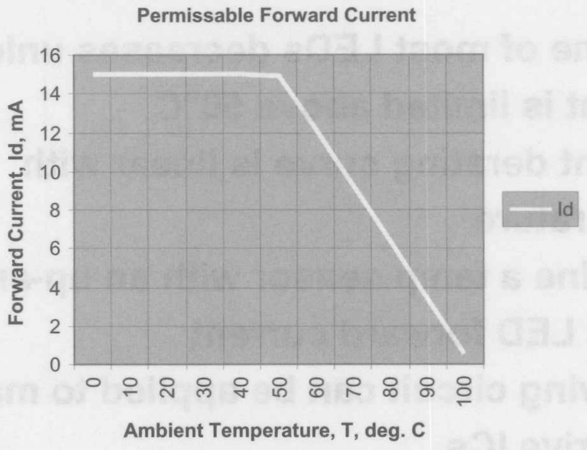
Current/Temperature Constraints Driving LEDs

- Lifetime of most LEDs decreases unless current is limited above 50°C
- Current derating curve is linear with temperature
- Combine a temp sensor with an op-amp to adjust LED forward current
- Following circuit can be applied to many LED drive ICs

Most LED manufacturer's datasheets provide detailed information regarding LED life with respect to temperature and forward current. In general, the larger the average forward current, the more aggressive the current derating must be as ambient temperature increases. Lifetimes of the devices are guaranteed only if these current derating curves are followed. For example, the LW-E67C Power TopLED® from Osram Optosemiconductor can safely withstand the rated 30mA of forward current for ambient temperatures up to 55°C. (The device is rated to operate from –40 to +100°C) In order to survive a minimum of 10,000 hours the current must be de-rated linearly from 30mA at 55° to 0mA at 100°C. Osram provides a second curve which guarantees a 5,000 hour life which derates forward current with the same slope beginning at 30mA for 65°C and continuing down to 7mA at 100°C.

Long life for LEDs is especially important as manufacturers replace incandescent lamps in automobile tail-light and turn signals with LED arrays. With lifetime guaranteed to 10,000+ hours the arrays can be built into the lamp module, with no expectation of replacement during the vehicle lifetime.

LED Current Derating Curve



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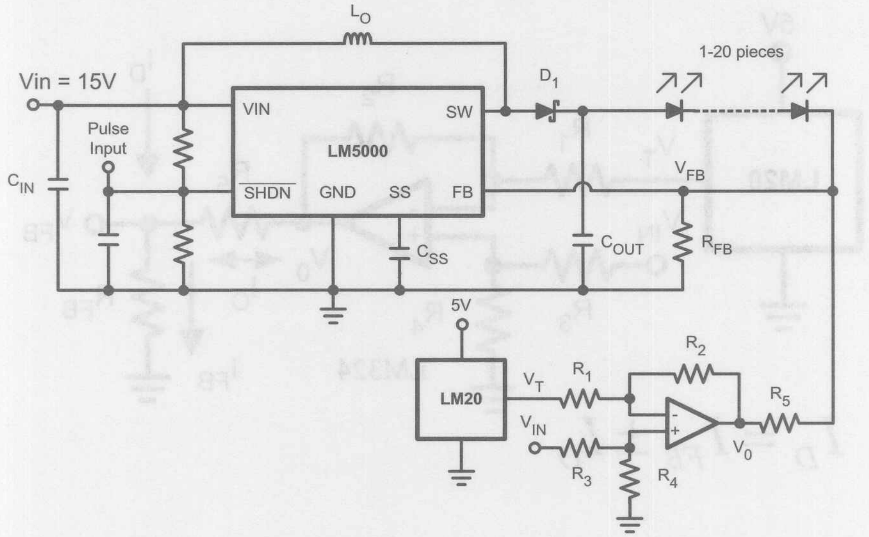
The Art of Analog 44

The curve in the graph represents the current derating needed to guarantee a 10,000+ hour life for a low-power GaN-based white LED. A typical package for this device would be the P-LCC-2 which has the same footprint as a 1210 size resistor or capacitor. The full rated current of 15mA can flow through the LED (or string of LEDs) as long as the ambient temperature is 50°C or less. Above 50°C the current decreases linearly, at a rate of 1/3 of a milliamp per degree Celsius. At 100°C the LED cannot carry any current without risking a shortened lifespan.

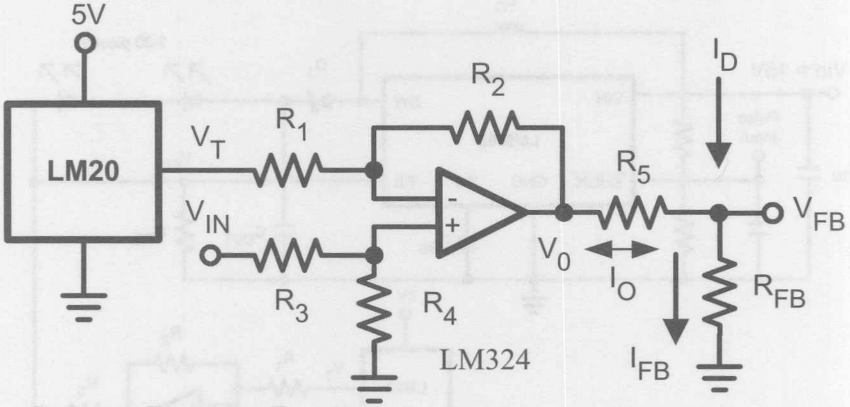
Temperature Compensated Circuit



As shown in this circuit, the output of the LM20 (a negative coefficient, CMOS temp sensor) is fed into a low cost op-amp in a differential configuration. The op amp can be almost any single-rail device, such as the LM324, or LM358. Vo, the output of the differential amplifier, sinks additional current through the op-amp at a user-selected level. As temperature increases, the op-amp sinks less and less current, and then begins to source current into the feedback node, lowering the percentage of feedback voltage generated by the LED string current. This continues until the current in the LED string reduces to zero.

One constraint of this design is that it requires the op-amp to sink and source milliamp range currents. For a 15mA design this is not a problem, however in applications with high current LEDs, like the Osram Golden Dragon® LED which takes 400mA average forward current, a different topology would be needed.

Diff Amp/LM20 Design Details



$$I_D = I_{FB} \pm I_O$$

The current through the LED string, Id, is governed by Kirchoff's Current Law. Without the temperature adjusting circuit, Vfb would be equal to Ifb*Rfb. By adjusting Io with respect to temperature, the feedback voltage (1.28V for the LM5000) is maintained even as Id drops to zero. This circuit can be used to adjust almost any switching regulator that is being operated in constant-current mode. A spare op-amp (the LM324 comes in a quad configuration) can be used to buffer the output of the LM20 if R1 is not high enough in resistance.

Because the operating current of the LM20 is so low (10 µA max over temp) the 5V supply can be created with a simple resistor divider as long as the input voltage does not vary too widely. In the case of a car battery, even a discharge great enough to cause a drop in input voltage to 8V should not disturb the operation, as the LM20 can operate from as little as 2.4V in.

Current Adjustment

- Op Amp output is lower limit (about 0.6V for LM324) for T 50°C, so current is constant
- For T = 50°C and above, LED current Id drops off linearly
- At T = 100°C Id ð 0

$$I_d = \frac{V_{FB}}{R_{FB}} + \frac{V_{FB} - V_O}{R5}$$

If the op amp were able to swing below zero volts at the output, the LED current would increase beyond the desired 15 mA maximum for temperatures below 50°C. This circuit takes advantage of the normal characteristic of single-rail operation: the op-amp cannot output less than the saturation voltage of the output stage (approximately 0.6V for the LM324). If an op amp other than the LM324 is used, the compensation circuit must be re-calibrated to reflect the new saturation voltage.

Component Selection

- **Select nominal current (ex. 15mA)**
- **Select Rfb and R5 assuming Vo = 0.6V (for LM324) (ex. Rfb = 100Ω, then R5 = 309Ω 1%)**
- **Select high value for R1 (to avoid loading the LM20) Find output voltage of LM20 at the engage point (T=50°C, Vt = 1.2792V)**
- **Suggestion: create spreadsheet!**

The differential amplifier in a non-balanced bridge presents a transfer function with four independent variables. An easier way to select the components is to put the equations into a spreadsheet and set the current (Rfb and R5) then set the inverting gain (R1 and R2) and finally the offset (R3 and R4) in sequence. Again, a spare op-amp could be put to use buffering the output of the temp sensor if desired.

Component Selection Cont'd

5. **Plug transfer function of differential amp and set gain by trial and error**

$$V_O = \frac{R4}{R1} * \frac{R1 + R2}{R3 + R4} * V_{IN} - \frac{R2}{R1} * V_T$$

- **Ex. R2 = 2.43M sets Id to 15m A**

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A good starting point here is to set R1 to 330 kΩ (if there is no buffer) and set R2 to 3.3 MΩ for an initial gain of 10.

Component Selection Cont'd

- **Set Vo, the output of the differential amp, to 0.6V with R3 and R4**

Ex. After trial and error: R3 = 115kΩ , R4 = 10kΩ

R3 and R4 form a voltage divider which offsets the differential amplifier. A good starting point is to select them so that the voltage at the non-inverting terminal is equal to the LM5000 feedback voltage:

R4 = 10 kΩ , then R3 by the voltage divider formula = 10.7*R4

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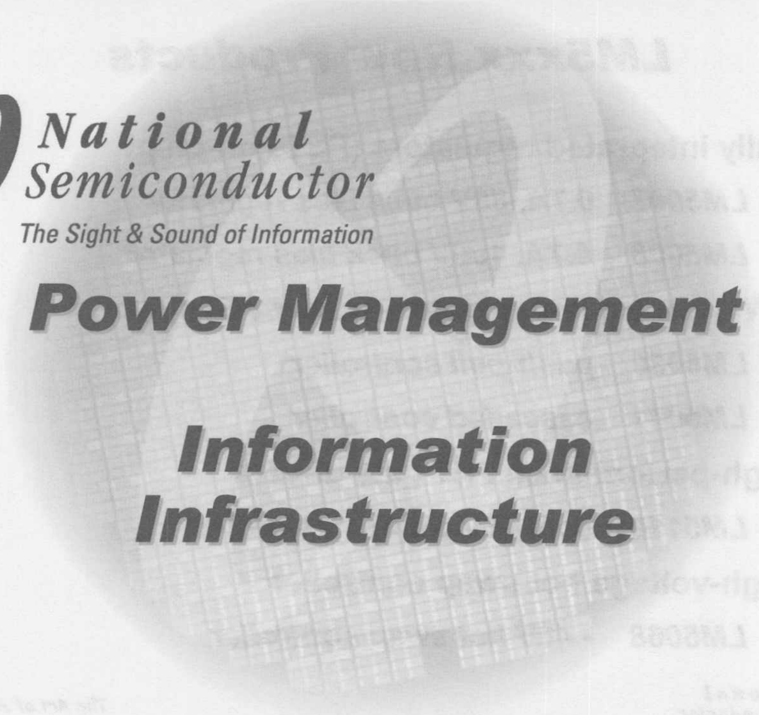
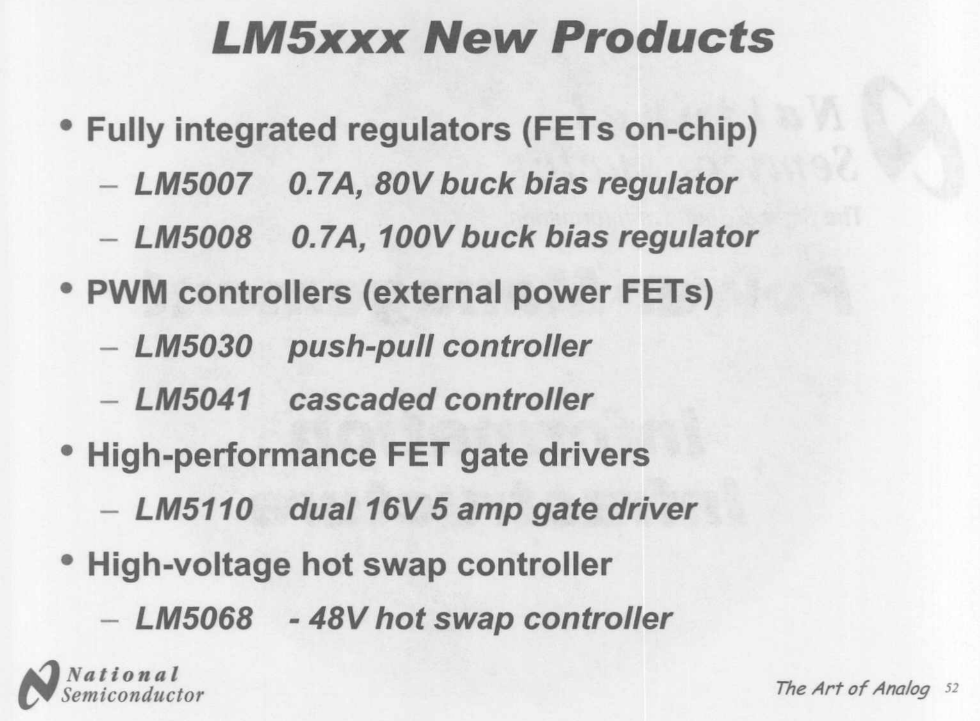


Power Management

Information Infrastructure



LM5xxx New Products

- Fully integrated regulators (FETs on-chip)
  - *LM5007 0.7A, 80V buck bias regulator*
  - *LM5008 0.7A, 100V buck bias regulator*
- PWM controllers (external power FETs)
  - *LM5030 push-pull controller*
  - *LM5041 cascaded controller*
- High-performance FET gate drivers
  - *LM5110 dual 16V 5 amp gate driver*
- High-voltage hot swap controller
  - *LM5068 - 48V hot swap controller*

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This segment presents information on a new family of products which enable the designer to create cost-effective switching power supply solutions for a variety of applications.

The LM5007/8 are fully integrated (N-FET on chip) buck converters which can function with input voltages as high as 80V and 100V, respectively. They have simplified control schemes which require no external compensation.

We also offer a family of controller IC's designed to drive external FET's in the LM5030 and LM5041 which address different switching converter topologies.

The LM5110 is a high-side gate driver IC which provides the level shifting (boosting) of gate drive voltage required to drive the top-side N-FET in a standard synchronous buck switching converter, as well as adding some other features.

Hot-swap controller designs are simplified using the LM5068, with internal surge current limiting and built-in protection features.

LM5007/8 High Voltage Step Down Switching Regulator

Features

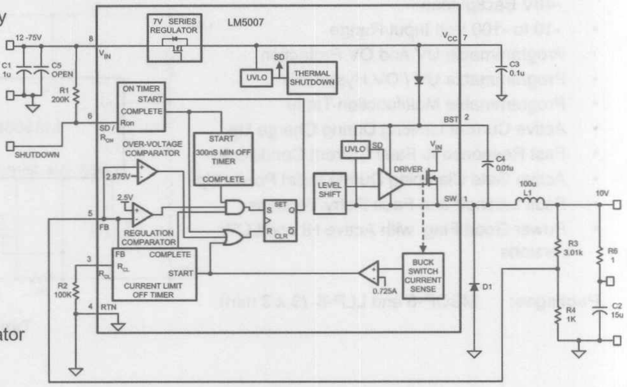
- Integrated 80V or 100V N-Channel Buck Switch
- Internal HV Start-up Vcc Regulator
- No Control Loop Compensation
- Nearly Constant Switching Frequency with Varying Line Voltage
- Adjustable Output Voltage
- Highly Efficient Operation
- Precision Reference (2.5V)
- Low Bias Current (350uA, typ.)
- Intelligent Current Limit Protection
- Thermal Shutdown

Package

MSOP - 8 and
LLP - 8 (4mm x 4mm)

Typical Applications

- Non-Isolated Buck Regulator
- Secondary High Voltage Post Regulator
- +42V Automotive System Regulator



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Low-cost step down converters can be easily implemented using the LM5007/8, a switching regulator controller which also contains an internal N-FET rated for 80v (LM5007) or 100V (LM5008). These devices do not contain an oscillator, the controller operates using a fixed ON time topology, with the ON time being dependent on both input voltage and an external resistor. FET switch ON time is inversely proportional to the input voltage. In this way, the inductor current is continuous and the switching frequency remains relatively constant. There are very few external components needed for the application, and the device requires no loop compensation yet still delivers very fast transient response.

The internal current limiter is set to 0.725A peak. Intelligent current limit is employed which causes the FET switch to be turned off for a period of time whenever the limit threshold is reached on any switching cycle. Because the "OFF" time is inversely proportional to output voltage, there is less limiting action at higher output voltages allowing fast response to load transients but still providing low average current when the output is severely overloaded or shorted (which forces the voltage at the FB pin down).

Target applications for these devices are non-isolated buck converters operating from input voltages up to 100V. The key advantages built into the part are that it requires no loop compensation, maintains a constant switching frequency over line variation, and has a built-in 7V "start-up" regulator which powers the device.

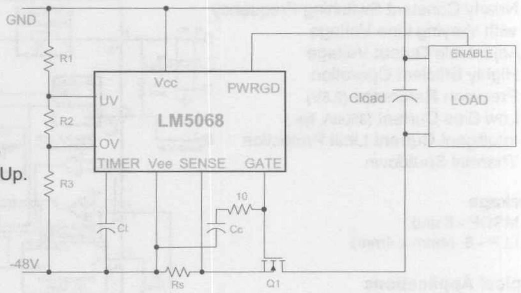
A precise (2%) internal 2.5V reference is built into the LM5007/8 to allow setting the output voltage along with two external resistors. To minimize drain from the input source and keep power dissipation low, the devices operate from very little bias current (350 uA typical).

LM5068 Hot Swap Controller

Features

- Safe Module Insertion and Removal from Live -48V Backplanes
- -10 to -100 Volt Input Range
- Programmable UV and OV Protection
- Programmable UV / OV Hysteresis
- Programmable Multifunction Timer
- Active Current Limiting During Charge Up
- Fast Response to Fault Current Conditions
- Active Gate Clamping During Initial Power Up.
- Fault Latched and Fault Retry Versions
- Power Good Flag with Active HI and LOW Versions

Packages: MSOP-8 and LLP-8 (3 x 3 mm)



Typical Application Circuit

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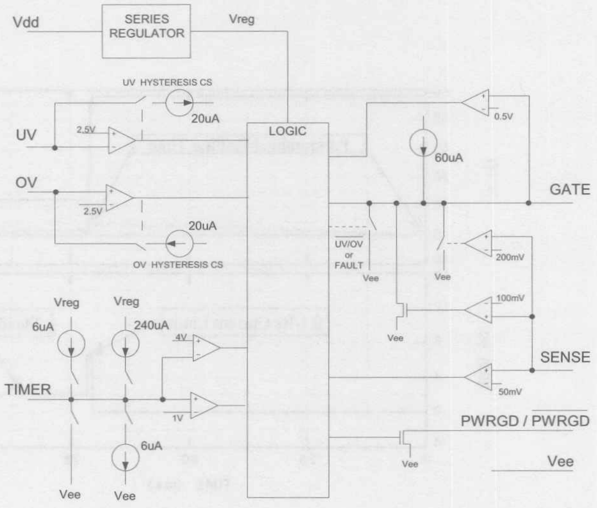
Hot-swap controlled power supplies are those which can be "swapped out" without turning off the input power. This is essential in systems which must remain under power at all times, even when units are removed for service. Many telecom and datacom systems are configured from subsystem racks and chassis, each containing a system host or controller card, one or more power supplies, and various subassembly cards performing functions of data processing, data transmission and switching. The interconnect between the different modules is often accomplished with a backplane or motherboard. Power is commonly provided to the various module slots via a –48V distribution bus.

National's first Hot Swap IC is the LM5068, and is ideally suited for –48V input voltage applications. The device limits inrush currents when the application card is plugged into the back plane. After the application board is plugged, in the IC continues to monitor the load current. If an over-current is detected the device will disconnect the load from the back plane.

The device comes in two varieties, one which shuts down and latches off after a fault is detected, and another which "retries" after a wait time. The multi-function timer pin serves three timing functions. First, after the card is plugged in a period of time is allowed for the signals to settle before the external pass element (Q1) is turned ON. The second timer function determines the amount of time to wait after an over-current is detected before a shutdown is commenced. The timer's third function is the amount of time to wait before a "retry" following a fault detection and shutdown. (fault retry version only).

Additional features include line Under/Over voltage shutdown with programmable hysteresis. Also an open drain Power Good indicator is provided. This Power Good signal is available as either an active low or an active high.

LM5068 Functional Blocks



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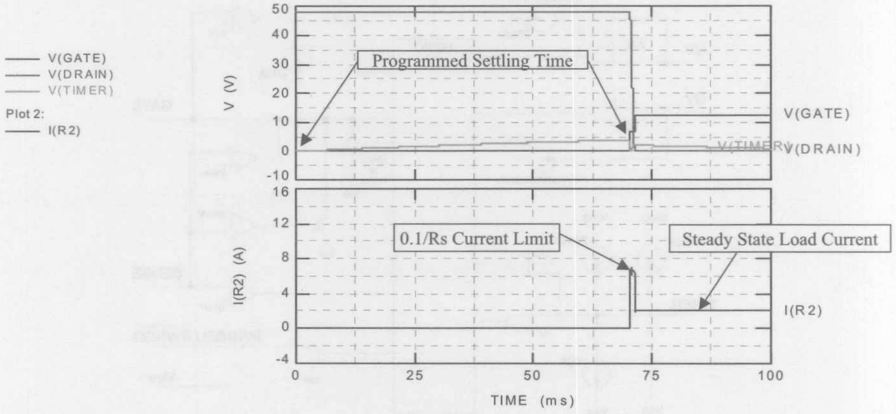
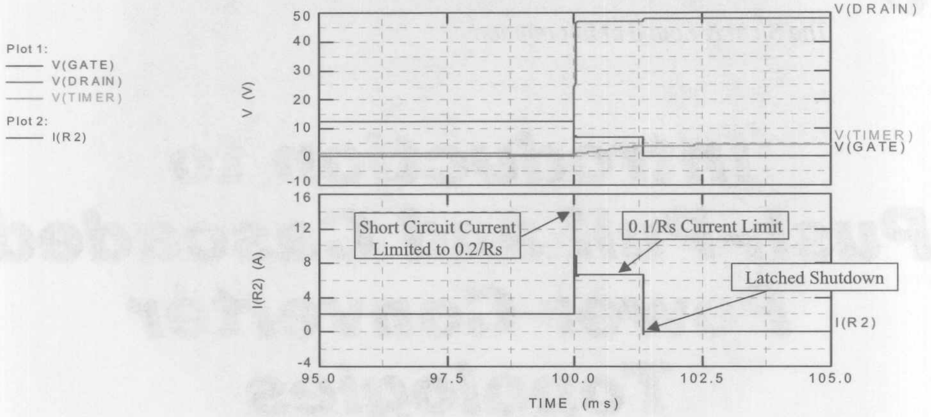
The UV/OV comparators have a 2.5V threshold. If either detects an OV or a UV fault condition, a 20 uA current source either sinks or sources current into the pin, which provides hysteresis. The sense pin monitors the voltage across a current sense resistor. If a voltage greater than 50 mV is detected, the timer capacitor starts to charge from a 240 uA current source. If the timer capacitor reaches 4V, a fault is declared. If the voltage on the sense pin reaches 100 mV, the gate output is reduced in a closed-loop fashion to limit the sense voltage to 100 mV. In the event of an abrupt short circuit, the 100 mV loop may overshoot causing the sense voltage to exceed 100 mV. If the sense voltage reaches 200 mV, a fast comparator trips and discharges the gate allowing the 100 mV loop to catch up. The power good signal is initiated when the gate voltage exceeds 10 Volts.

LM5068 Normal Turn-On



The waveform shown represents a simulation of a normal hot-plug turn-on event. The initial turn-on delay allows settling of the mated contacts. Following the settling time delay, the external MOSFET is enabled. The analog limiter loop limits the inrush current to 100 m/Rs. Once the load capacitor is charged, the load current is then the steady state current and the gate rises to saturation (approximately 12V).

LM5068 Short Circuit Response



Short Circuit Current Limited to 0.2/Rs

0.1/Rs Current Limit

Latched Shutdown

This simulation shows what occurs during a short-circuit fault event. Because of the output short, the load current shoots high and trips the 200 mV fault sense comparator. The gate is immediately pulled down. The 100 mV loop limits the load current. During this entire period of time the timer capacitor is charging. When the timer voltage gets to 4V, a fault is declared and the device shuts off. The latched version will remain off until power is recycled. The retry version will charge and discharge the timer capacitor 8 times, with a small current. After the 8 timer cycles, a retry will be attempted.

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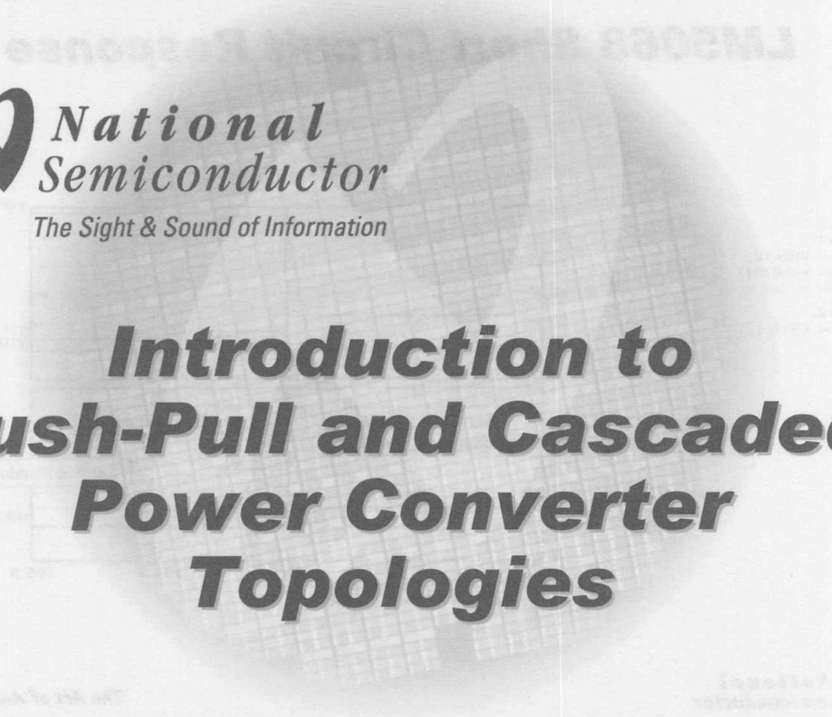
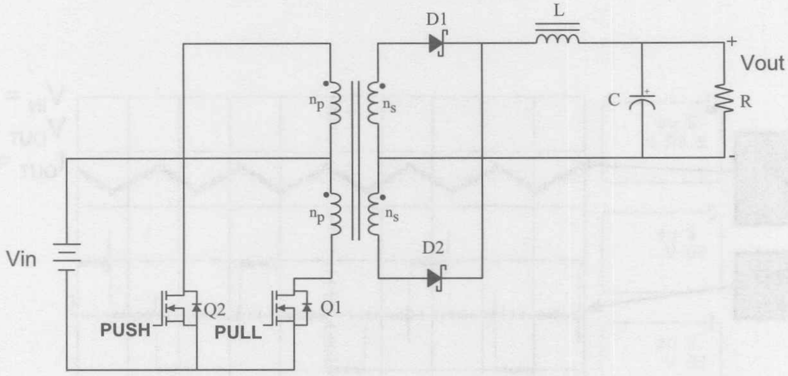
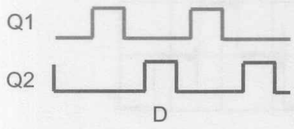


Introduction to Push-Pull and Cascaded Power Converter Topologies

This segment is a brief tutorial which defines and explains push-pull converters and covers the use of "cascading" different converter topologies for achieving specific design objectives.

Push-Pull Topology





$$\boxed{V_{out} = V_{in} \times D \times \frac{N_s}{N_p} \times 2}$$

The Push-Pull topology is basically a specific type of forward converter. The name "push-pull" comes from the fact that the center tap of the primary winding (connected to Vin) effectively creates two primary windings which are energized on alternate switching cycles.

A switch is connected to either end of the winding, and they pull that end to ground on alternate switching cycles (forcing the Vin voltage across each half winding depending upon which switch is turned on).

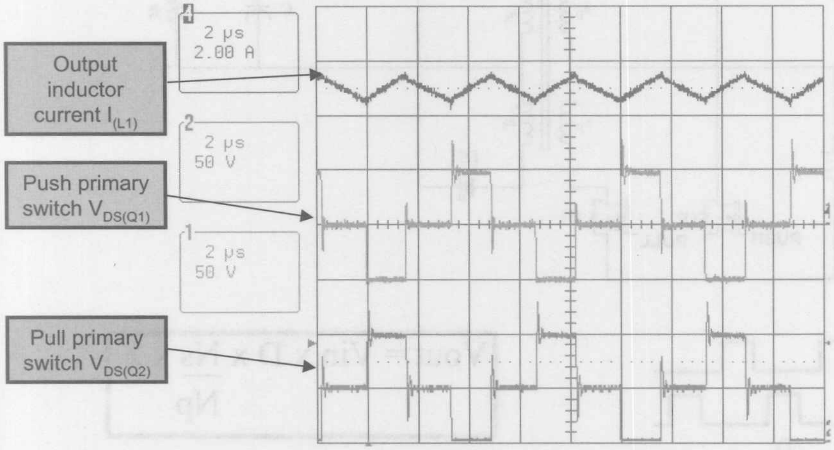
A push-pull is in the converters classified as "forward" converters, meaning that transformer primary and secondary current flow at the same time. When Q1 is ON, current flows through D1. When Q2 is ON, current flows through D2.

The secondary winding is arranged in a center-tapped configuration as shown. Because of this, the switching pulses reaching the output filter are twice the frequency of either Q1 or Q2.

The transfer function of the push-pull (shown above) is similar to the forward converter, where "D" is the duty cycle of either primary winding, which is why there is an "X2" term.

When neither Q1 nor Q2 is active, the output inductor current splits between the two output diodes. A transformer reset winding, sometimes used in other forward converter topologies, is not necessary in a push-pull, because the core is reset on every switching cycle.

Push-Pull Switching Waveforms



Output inductor current $I_{(L1)}$

Push primary switch $V_{DS(Q1)}$

Pull primary switch $V_{DS(Q2)}$

$V_{IN} = 48V$

$V_{OUT} = 3.3V$

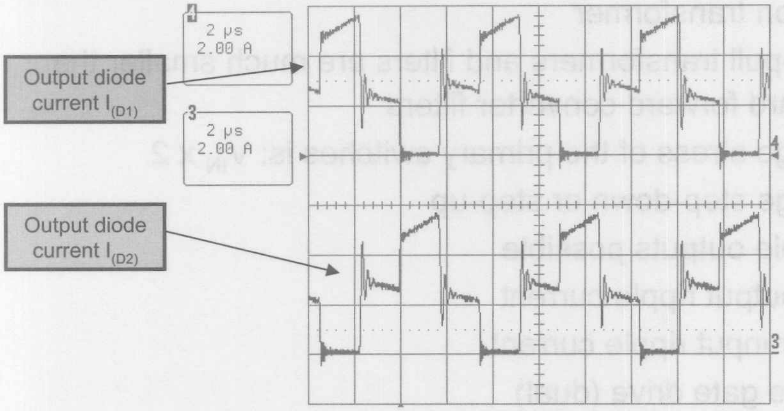
$I_{OUT} = 5A$

This figure shows the oscilloscope waveforms for the Drain voltages of the two primary switches and the output inductor current.

When a given primary is active, the corresponding switch Drain voltage is zero and the alternate switch Drain voltage is 2X the input voltage, due to the transformer voltage being "reflected" from the active primary to in-active primary. This is a known characteristic of push-pull designs: the switches must be able to withstand at least twice the maximum input voltage to safely operate.

When neither switch is turned ON, both Drain voltages are held at the input voltage level.

Push-Pull Diode Currents



V_{IN} = 48V
V_{OUT} =3.3V
I_{OUT} = 5A

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This oscilloscope photo shows the currents flowing in the output diodes. These two currents sum to form the output inductor current shown on the previous slide. When neither of the primary switches are ON, the output inductor current has a negative slope and flows half in each of the two secondary diodes.

Push-Pull Characteristics

- A push-pull converter uses a dual-drive primary winding isolation transformer
- Push-pull transformers and filters are much smaller than standard forward converter filters
- Voltage stress of the primary switches is: V_{IN} x 2
- Voltage step-down or step-up
- Multiple outputs possible
- Low output ripple current
- Lower input ripple current
- Simple gate drive (dual)
- Large achievable duty cycle range

A Push-Pull converter uses a dual-drive-winding isolation transformer, in which either primary winding is powered during alternate switching cycles. As long as the alternate half cycles are symmetrical, the transformer is self resetting. Push-Pull inductors and output capacitors are much smaller than standard forward converter filters, because the frequency pulses being filtered by the output L-C filter are twice the switching frequency of either FET switch.

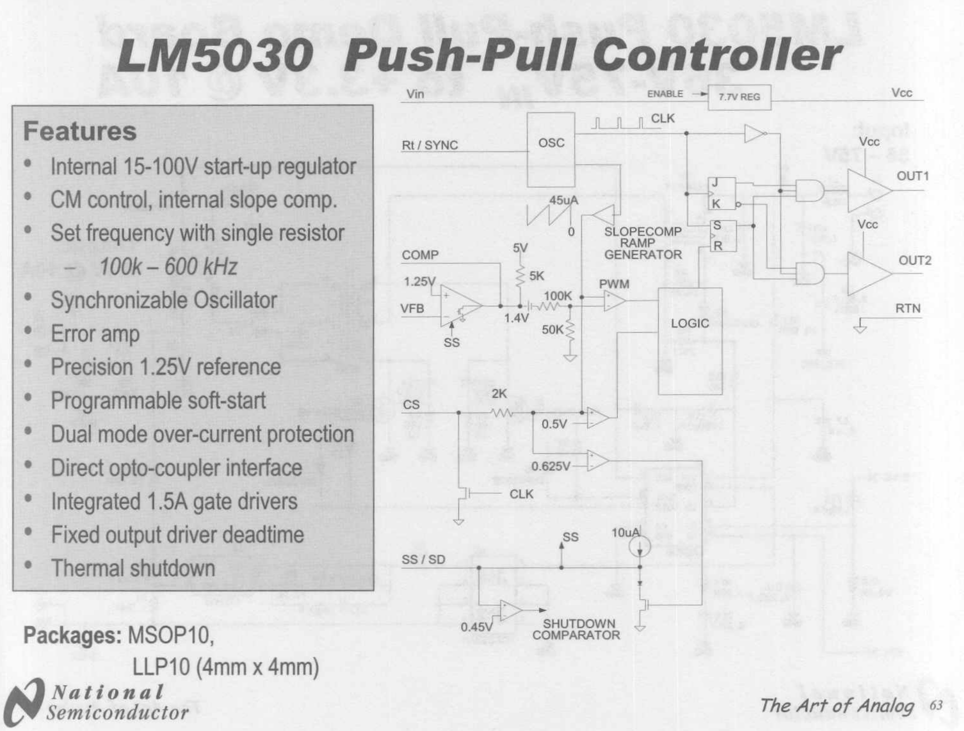
Voltage Stress of the Primary Switches is: Vin x 2, due to the reflected transformer voltage. For this reason, push-pull converters are generally more attractive at lower input voltages.

The push-pull can easily be used to either buck (step-down) or boost (step-up) because all it requires is to change the turns ratio on the transformer. Multiple outputs can be easily implemented by simply adding more secondary windings and output stages.

Because both N-FET switches are ground referenced, gate drive is much simpler and requires no "high side" boosting to get sufficient gate drive voltage.

Output ripple current is generally lower for a given size of filter components, because of the doubling in frequency of the secondary waveform pulses reaching the output filter.

Input ripple current is generally lower because the push-pull more efficiently utilizes the input voltage and can operate to almost 100% effective duty cycle.



LM5030 Push-Pull Controller

Features

- Internal 15-100V start-up regulator
- CM control, internal slope comp.
- Set frequency with single resistor
  - 100k – 600 kHz
- Synchronizable Oscillator
- Error amp
- Precision 1.25V reference
- Programmable soft-start
- Dual mode over-current protection
- Direct opto-coupler interface
- Integrated 1.5A gate drivers
- Fixed output driver deadtime
- Thermal shutdown

Packages: MSOP10,
LLP10 (4mm x 4mm)

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The LM5030 is a controller IC designed for current-mode control converters which utilize alternating outputs such as push-pull, half-bridge, and full-bridge converters. Because of CM control, it offers all the advantages such as: simplified loop compensation, cycle-by-cycle current limiting, and fast line response from feed-forward compensation.

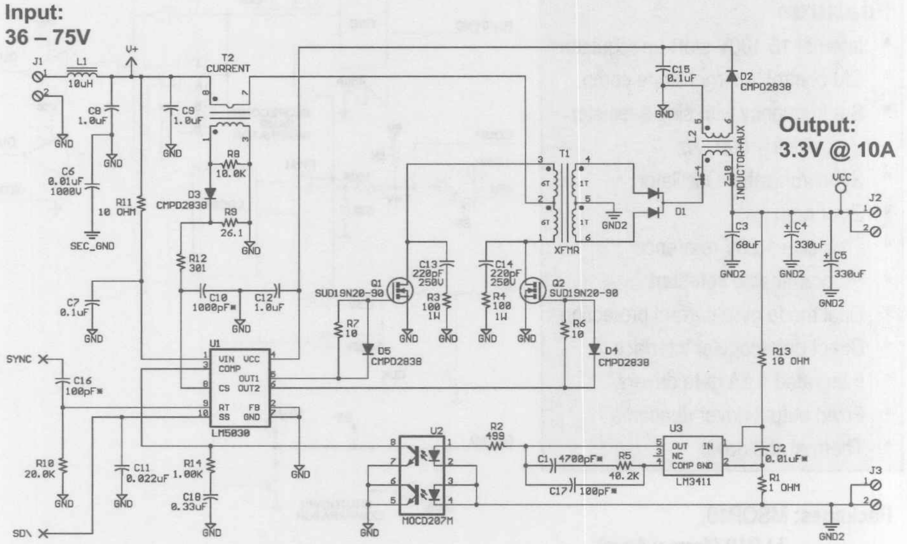
An internal start-up regulator is provided which down regulates Vin to 7.7V for internal power, allowing the input pin (Vin) to be connected directly to line voltages as high as 100V. The output of this regulator is internally current limited to 10 mA. Upon power up, the regulator is enabled and sources current into an external capacitor connected to the Vcc pin. When the voltage on the Vcc pin reaches the regulation point of 7.7V, the controller outputs are enabled. In typical applications, an auxiliary transformer winding is diode connected to the V_{CC} pin. This winding raises the Vcc voltage greater than 8V, effectively shutting off the internal startup regulator and saving power while reducing the controller dissipation. The external Vcc capacitor must be sized such that the self-bias will maintain a V_{CC} voltage greater than 6.1V during the initial start-up. An external start-up or other bias rail can be used instead of the internal start-up regulator by connecting the Vcc and the Vin pins together and feeding the external bias voltage (8 – 15V) into that node.

The LM5030 oscillator is set by a single external resistor connected between the RT pin and return. The programming range is 10 KHz to 1 MHz. The oscillator frequency is specified at two points in the electrical table 100 KHz and 600 KHz. The internal oscillator can also be synchronized to an external clock. The external clock must be of higher frequency than the free running frequency set by the RT resistor. The clock signal should be capacitively coupled into the RT pin with a 100 pF capacitor. A peak voltage level greater than 3 Volts is required for detection of the sync pulse. The sync pulse width should be set in the 15 to 150 nS range by the external components. The RT resistor is always required, whether the oscillator is free-running or externally synchronized.

Two levels of over-current protection are incorporated into the LM5030. If the voltage at the CS input exceeds 0.5 Volts the present output cycle is terminated (cycle by cycle current limit). If the voltage at the CS input exceeds 0.625 Volts, the controller will terminate the present cycle and discharge the soft-start capacitor. A small RC filter, located near the controller, is recommended for the CS pin. An internal MOSFET discharges the current sense filter capacitor at the conclusion of every cycle, to improve dynamic performance.

The internal drivers for the two alternating outputs two alternating outputs, OUT1 and OUT2, can each source 1.5A peak.

LM5030 Push-Pull Demo Board
36V-75V$_{IN}$ to +3.3V @ 10A



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The Art of Analog 64

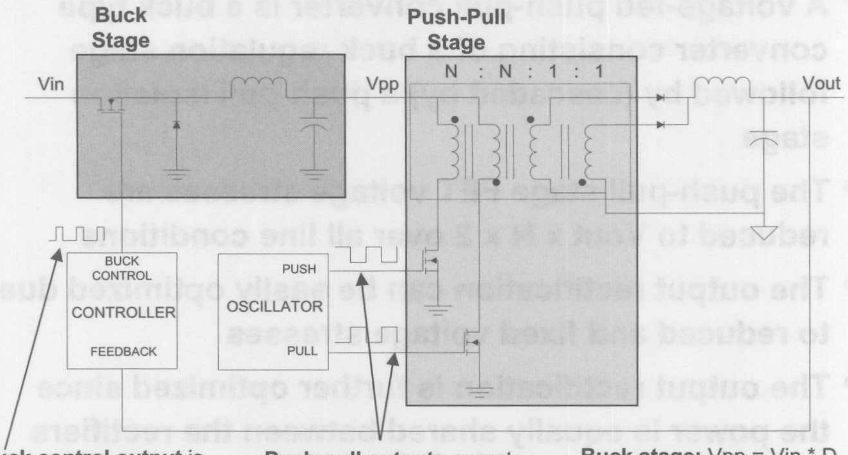
A demo board is available from NS which shows the LM5030 in a 33W push-pull design.

In this design, the controller connects directly to the input voltage to provide the initial bias power on V_{CC}. The primary/input and the secondary/output grounds are fully isolated, which is important for safety and noise reduction reasons. The LM5030 is designed for either isolated or non-isolated applications. In non-isolated applications the power converter output is connected to the VFB pin via the voltage-setting resistors and loop compensation is connected between the COMP and VFB pins. For most isolated applications, the error amplifier function is implemented on the secondary side ground. Since the internal error amplifier is configured as an open drain output it can be disabled by connecting VFB to ground. The internal 5K pull-up resistor, connected between the 5V reference and COMP, can be used as the pull-up for an optocoupler or other isolation device. An opto-coupler is used to send a regulation error signal across the ground boundary. The LM3411 monitors the output voltage and compares it to a precision internal reference. The difference between the output voltage and the reference form the error signal used to increase or decrease the primary switches duty cycle in order to regulate the output.

The four magnetic devices utilized in the design are the Power Transformer (T1), Input Filter Inductor (L1), Output Filter Inductor L2 and the Current Sense Transformer (T2). The power transformer is arranged in a center-tapped configuration on both the primary and the secondary. There are 12 turns on each primary winding and 2 turns on each secondary winding. The input inductor, L1 works with the input capacitors C8, C9 to reduce input ripple current. The output filter provides the filtering for the output voltage and also there is a small bias winding wound on the inductor core which acts as a transformer winding to create a bias voltage to power the controller. Upon power up, the controller start-up regulator is enabled and sources current into the V_{CC} capacitor C12. This winding raises the V_{CC} voltage greater than 8V, effectively shutting off the internal startup regulator and saving power while reducing the controller dissipation.

The current sense transformer T2 is used to measure the current in each of the primary switches, which is used in the controller for current-mode control and for over-current protection.

Cascaded Buck & Push-Pull Power Converter (Voltage Fed)



Buck control output is pulse-width modulated to regulate Vout

Push-pull outputs operate continuously, alternating at almost 50% duty cycle

Buck stage: Vpp = Vin * D
Push-pull stage: Vout = Vpp / N
Overall: Vout = Vin x D/N

The circuit shown combines the buck topology and the push-pull converter. In this particular case, each switch of the push-pull stage is set to operate alternating at approximately 50% duty cycle each, which means secondary current is flowing nearly 100% of the time. This configures the Push-Pull stage as a high-efficiency DC transformer. Any voltage presented to the Vpp node will be transferred to the output divided or multiplied by the transformer turns ratio.

The buck converter stage is PWM modulated to regulate the output voltage, with feedback from the Vout node being used to control the pulse widths of the buck converter.

The Push-Pull stage is said to be "Voltage Fed" since the Vpp node contains the output capacitor from the Buck Stage, so it looks like "voltage source" to the push-pull converter it is powering.

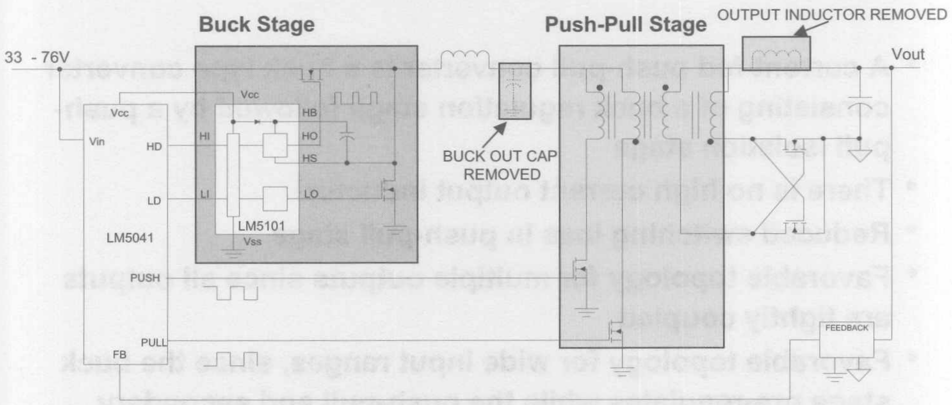
The Push-Pull switches actually operate slightly less than 50% duty cycle, because a slight "dead time" is required where both switches are off.

Cascaded Voltage-Fed Converter Benefits

- A voltage-fed push-pull converter is a buck type converter consisting of a buck regulation stage followed by (cascaded by) a push-pull isolation stage
- The push-pull stage FET voltage stresses are reduced to Vout x N x 2 over all line conditions
- The output rectification can be easily optimized due to reduced and fixed voltage stresses
- The output rectification is further optimized since the power is equally shared between the rectifiers over all load and line conditions
- Favorable topology for wide input ranges

Because the source voltage is bucked down before it is applied to the push-pull converter, the Push-Pull switch voltage stress is reduced which allows the use of lower voltage rated FETs with lower ON resistance which increase the converter efficiency.
The voltage stress on the output rectifiers (either diodes or FETs) is only Vout / 2 for this topology. Because the buck converter "pre-regulates" the input to the push-pull, this stress level is not proportional to the input line voltage as in a forward topology. The output rectifier stress for the forward topology is Vin x Ns/Np, where Ns is the transformer secondary turns and Np is the transformer primary turns. This fact allows use of lower voltage/higher current rated rectifiers which reduces cost and increases efficiency.
Because the Push-Pull stage operates at effectively 50% duty cycle per switch continuously, it follows that each of the output rectifier also operates continuously at 50% duty cycle for all operating conditions. This features ensures equal power dissipation and thermal stress for the two rectifiers.

Current Fed Push-Pull Concept



- Push and pull outputs operate continuously, alternating with a slight overlap.
- Output voltage is controlled by the buck stage which operates at 2x the push-pull frequency.
- Continuous output current from the push-pull stage requires minimal filtering.
- High efficiency achieved with low push-pull switching losses and matched sync rectifier loading

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The cascaded "Voltage Fed" buck and push-pull previously presented is a viable design approach, however there are several large components which can be removed, while still maintaining all of the performance benefits of the cascaded approach. On the previous Voltage-fed slide, note we had 2 complete L-C filters. The Buck Stage output capacitor and the push-pull stage inductor can be removed and actually provide several benefits.

Shown here is a current-fed cascaded buck and push-pull stage. The push-pull stage is said to be current fed since only the Buck inductor, which acts a current source, feeds the push-pull converter.

While it was the case in the previous example (which was voltage fed) that a small dead time was required where both switches were off, in the current-fed design it is necessary for both FET's to be on for a small overlap time period in order to provide a current path for the inductor current which can not stop abruptly.

With the example shown here, if the output voltage is 2.5V and transformer turn ratio is 8 to 1, the voltage at Vpp node will be 20V.

Cascaded Current-Fed Converter Benefits

- **A current-fed push-pull converter is a buck type converter consisting of a buck regulation stage followed by a push-pull isolation stage**
- **There is no high current output inductor!**
- **Reduced switching loss in push-pull stage**
- **Favorable topology for multiple outputs since all outputs are tightly coupled**
- **Favorable topology for wide input ranges, since the buck stage pre-regulates while the push-pull and secondary operate independently of the input voltage level**

A current-fed push-pull converter is a buck type converter consisting of a buck regulation stage followed by a push-pull converter which can serve as an isolation stage.

There is no high-current output inductor. All outputs share the single primary-based inductor.

In this case, the push-pull stage functions as a "current transformer" where the inductor current flowing in the inductor in the output of the buck stage is alternately channeled through either primary winding of the push-pull converter's transformer. The transformer allows this current to be increased or decreased via the transformer turns ratio, and the current flowing from the transformer secondary flows into the output capacitor from the secondary winding. The voltage at that point is used to control the pulse widths of the buck stage converter. The Push-Pull stage is switching at zero voltage; therefore switching loss is reduced.

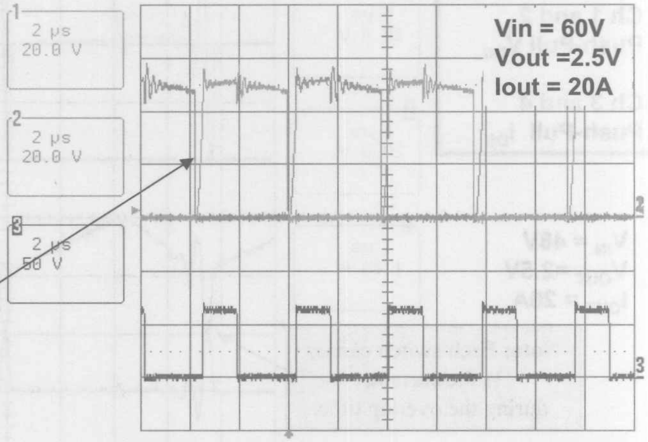
This is a favorable topology for multiple outputs since all outputs are tightly coupled. The capacitors from all of the outputs are effectively in parallel. The stress in the Push-Pull stage and the output rectifiers are independent of Vin, and that makes it also a favorable topology for application of wide input voltage ranges.

Current-Fed Switching Voltages

Trace 1:
Push_Pull SWPUSHV$_{DS}$

Trace 2:
Push_Pull SWPULL V$_{DS}$

Trace 3:
Buck Stage Switching Node



Vin = 60V
Vout =2.5V
Iout = 20A

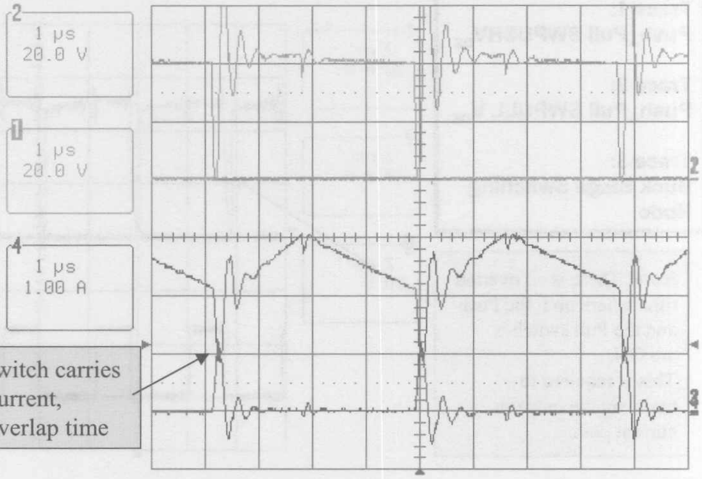
Note: There is an overlap time where both the Push and the Pull switches are ON.
This is required to maintain the inductor current path.

Shown here are scope plots of the push-pull stage drain voltages and the voltage at the common junction of the buck stage switches.
Note that the buck stage operates at twice the frequency of either the push or pull switch. Also note the overlap of the of the push-pull stage.

Current-Fed Push-Pull Switches

Ch 1 and 2
Push-Pull V_{DS}

Ch 3 and 4
Push-Pull I_{DS}

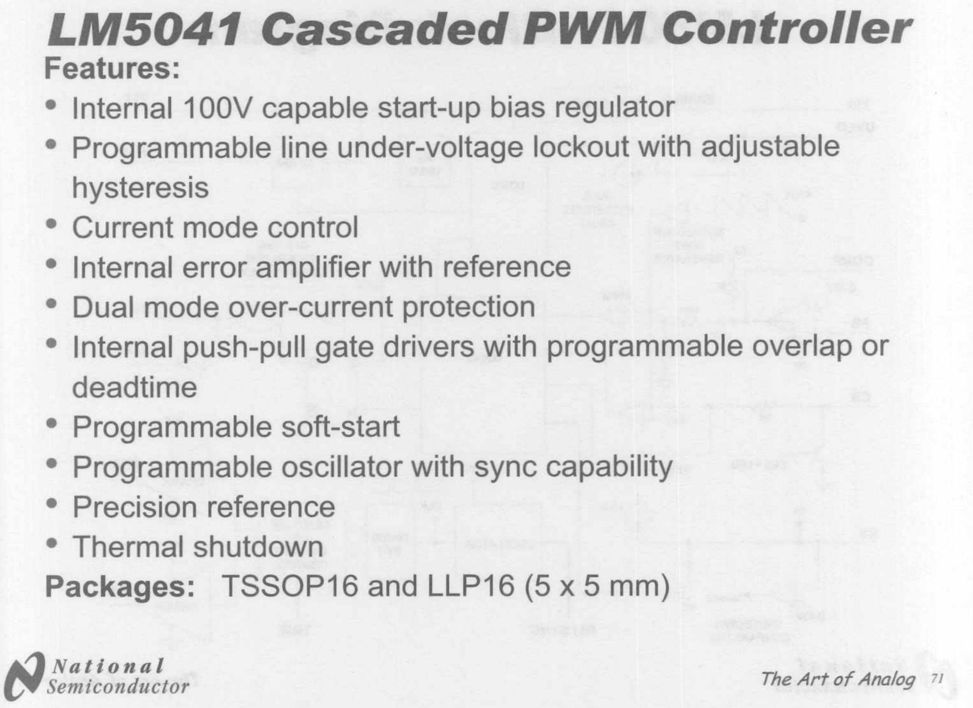


V_{IN} = 48V
V_{OUT} =2.5V
I_{OUT} = 20A

Note: Each switch carries
½ the current,
during the overlap time

Shown here are scope plots of the push-pull drain voltages and push-pull switch currents in the current-fed push-pull converter. One of the many advantages of this approach is a reduction in switching losses in the push–pull stage switches.

You can note during the overlap time when both switches are on, the buck inductor current divides equally between the two switches. At the conclusion of the overlap time the drain voltage is already at zero and therefore the switching losses are cut in half.



LM5041 Cascaded PWM Controller

Features:

- Internal 100V capable start-up bias regulator
- Programmable line under-voltage lockout with adjustable hysteresis
- Current mode control
- Internal error amplifier with reference
- Dual mode over-current protection
- Internal push-pull gate drivers with programmable overlap or deadtime
- Programmable soft-start
- Programmable oscillator with sync capability
- Precision reference
- Thermal shutdown

Packages: TSSOP16 and LLP16 (5 x 5 mm)

National Semiconductor

The Art of Analog 71

The LM5041 controller was developed to simplify designs of converters which utilize cascaded topologies. An internal start-up regulator (with built-in 15 mA current limit) can operate from inputs as high as 100V. Upon power application, the regulator is turned on and sources current into an external capacitor connected to the V_{CC} pin. When the voltage on the Vcc pin reaches the regulation point of 9V, the controller outputs are enabled. In typical applications, an auxiliary transformer winding is diode connected to the Vcc pin. This winding raises the V_{CC} voltage greater than 9V, effectively shutting off the internal startup regulator, improving efficiency and reducing the controller's power dissipation.

Current-mode control is used in the LM5041, yielding the benefits of simplfied loop compensation, cycle-by-cycle current limiting, and feed-forward compensation.

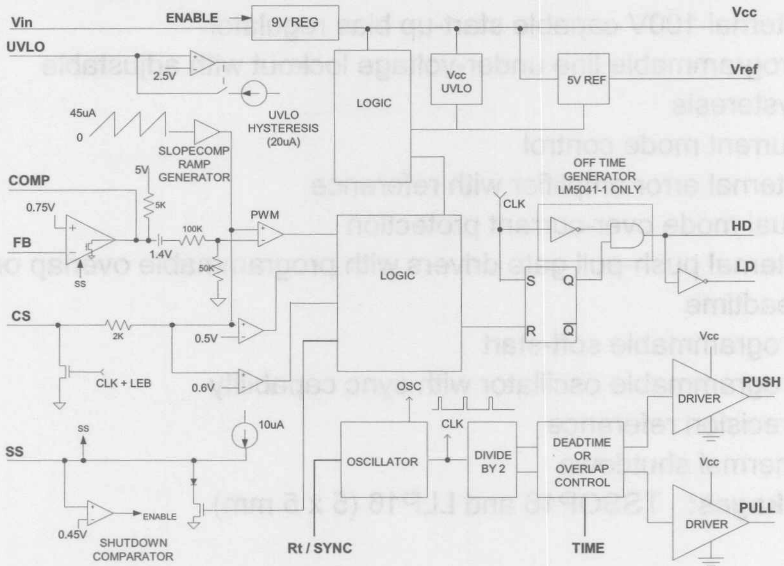
The LM5041 oscillator can be set from 10 kHz to 1 MHz by a single external resistor connected between the RT pin and return, with guaranteed operating points of 100 KHz and 600 KHz. The oscillator can also be synchronized to an external clock, operating at a higher frequency than the free running frequency set by the RT resistor. The clock signal should be capacitively coupled into the RT pin with a 100 pF capacitor.

Two levels of over-current protection are built into the LM5041. If the voltage at the CS input exceeds 0.5 Volts, the present output cycle is terminated (cycle-by-cycle current limit). If the voltage at the CS input exceeds 0.6 Volts, the controller will terminate the present cycle and discharge the soft-start capacitor. An internal MOSFET discharges the current-sense filter capacitor at the conclusion of every cycle, to improve dynamic performance.

The push-pull driver outputs operate continuously at a nominal 50% duty cycle. A distinguishing feature of the LM5041 is the ability to accurately configure either deadtime (both-off) or overlap time (both-on) on the complementary push-pull outputs. The overlap/deadtime magnitude is controlled by a resistor connected to the TIME pin on the controller. The other end of the resistor can be connected to either REF for deadtime control setting or GND for overlap control setting. Current-fed designs require a period of overlap to insure there is a continuous path for the buck inductor current. Voltage-fed designs require a period of dead time to insure there is no time when the push-pull transformer acts as a shorted turn to the low impedance sourcing node.

An internal high-gain error amplifier is provided within the LM5041, with the non-inverting input tied to 1.25V. The reference accuracy is 2% over the full temperature range (-40 to +105°C)

LM5041 Block Diagram



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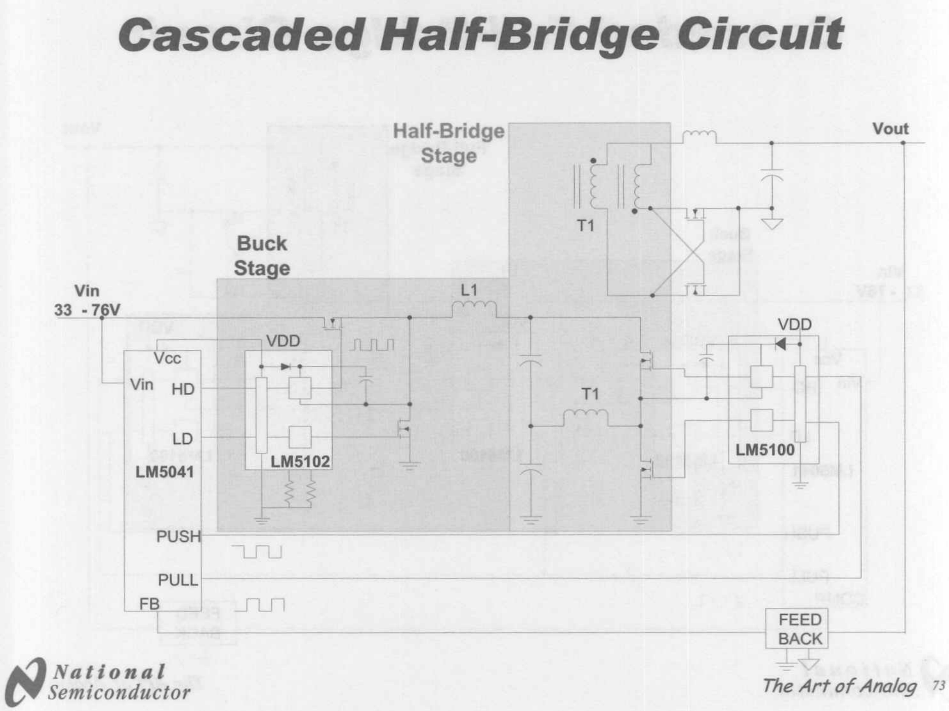
The Art of Analog 72

Built into the LM5041 cascaded controller are a total of 4 switch control outputs. Gate drivers are included within the device for the push and pull outputs. A resistor connected to the TIME pin is used to set either overlap or deadtime of the push-pull outputs. Connecting the resistor from the TIME pin to ground sets overlap time, while connecting the resistor from the TIME pin to the vref pin sets deadtime.

The buck-stage outputs are logic-level controls which work with national's new LM5100 family of buck stage gate drivers.

Some of the unique LM5041 features are a programmable line under-voltage lockout (UVLO) with adjustable hysteresis and also programmable soft-start.



Cascaded Half-Bridge Circuit

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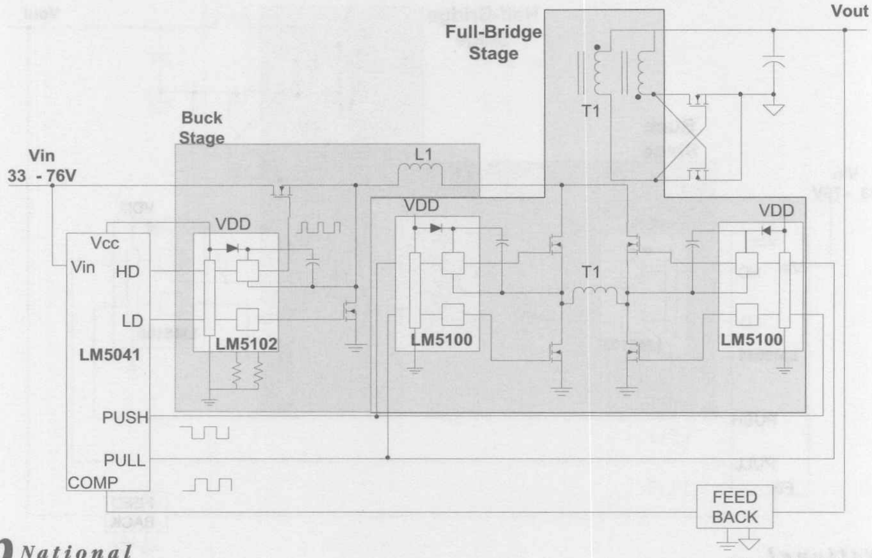
The Art of Analog 73

The Cascaded approach can be extended to many other switching converter topologies. Here a buck stage is cascaded with a half-bridge stage. In this case the Half-Bridge is said to be voltage fed, since the splitter capacitors on the output side of L1 are necessary for proper operation. This approach offers the benefit of further reduced voltage stresses on the primary side switches of (Vout X N) where N is the turns ratio, and a single primary winding.

Cascaded Full-Bridge Circuit



In this design, a buck converter is used to supply power to a full-bridge converter. The output capacitors after L1 are not required here, so this circuit is a “current-fed” design.

The benefits of this approach are:

•Reduced primary FET voltage stress of (Vout X N)

•Reduced switch current relative to the half-bridge

•Requires only a single primary winding.

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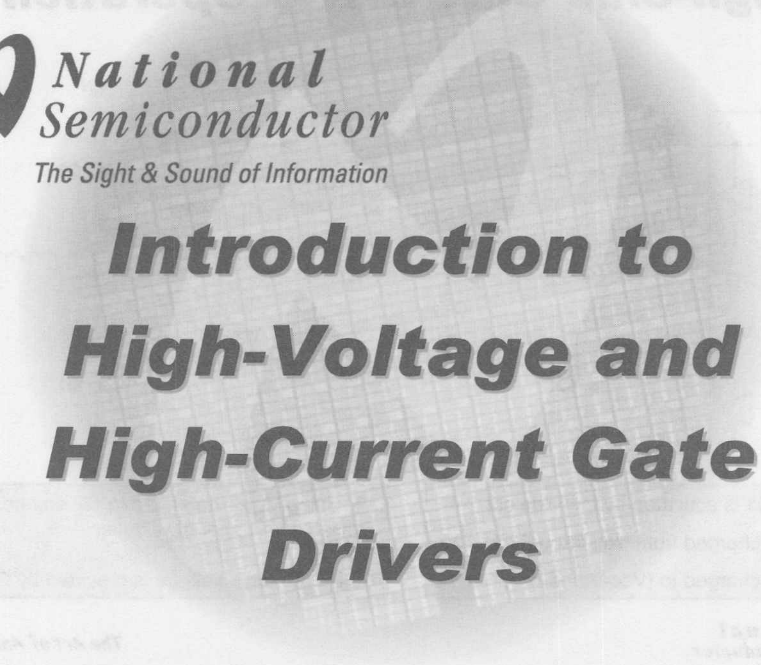


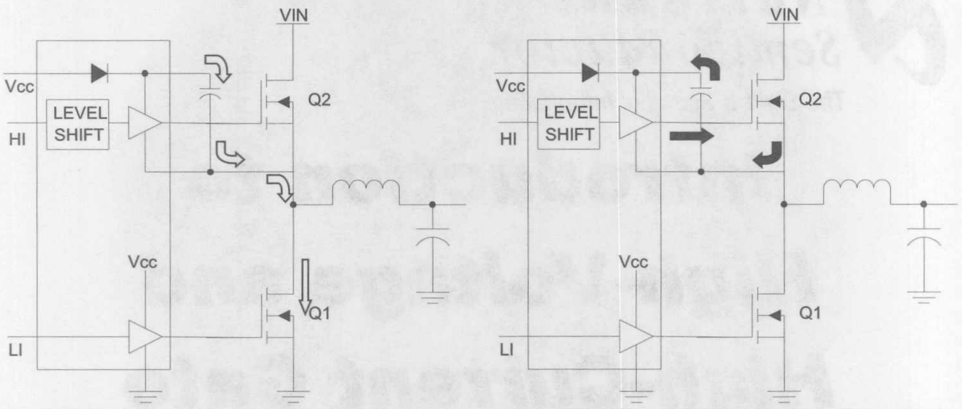
Introduction to High-Voltage and High-Current Gate Drivers

A common design chore required in all FET-based power converters is to come up with circuits that drive them. The key requirements of such drivers are:

They must be able to deliver high peak currents so that the gate capacitance can be charged quickly and create ultra-fast switching transitions.

They must provide the proper voltage level shifting as needed if high-side drive is required.

High-Side Gate Driver Operation



- Initially Q1 is activated by low side control
- Cboot is charged from Vcc through D1, Q1
- Cboot is charged to (Vcc-Vdiode)

- Floating Vcc, referenced to Q2 source, is available for upper gate driver
- Q2 Gate drive voltage is provided by Cboot

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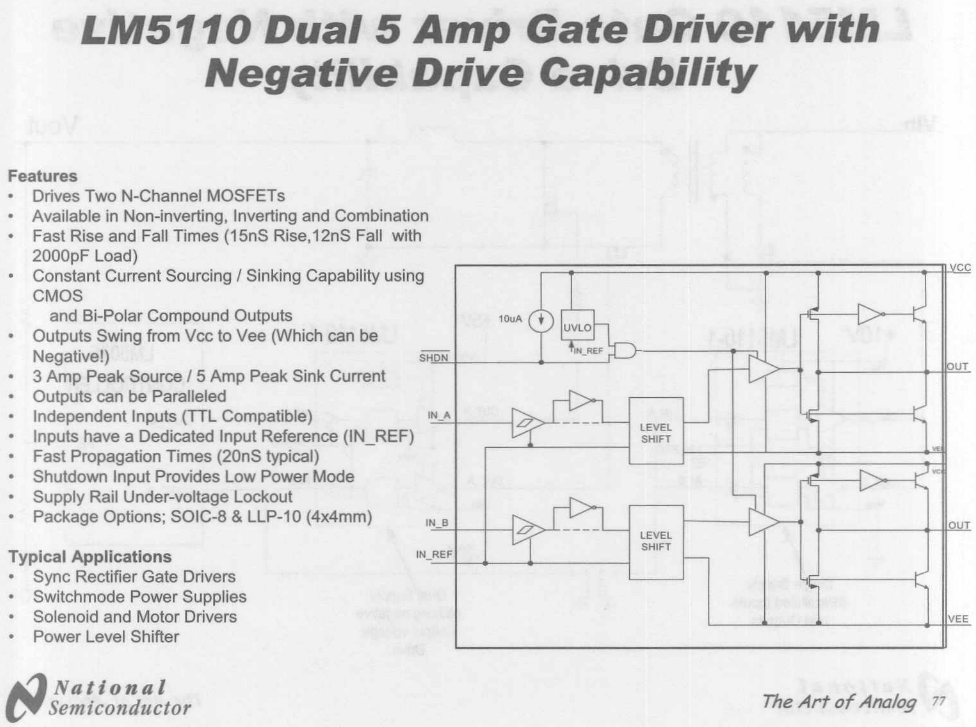
High-Side Gate Drivers are necessary to drive the Gate of the "top switch" used in any synchronous buck converter. Since that FET is riding above the regulated output, its gate must be driven higher to turn it on.

An effective way to do this is with a "Bootstrapping" technique:

In the left illustration, when a low side switch is ON, charge flows from Vcc to charge up a high side bootstrap capacitor. The charge on this capacitor is now available to drive the high side gate as shown on the right illustration.

National Semiconductor has developed a family of dual gate drivers with level shifter designed specifically for buck and bridge configurations.



LM5110 Dual 5 Amp Gate Driver with Negative Drive Capability

Features

- Drives Two N-Channel MOSFETs
- Available in Non-inverting, Inverting and Combination
- Fast Rise and Fall Times (15nS Rise,12nS Fall with 2000pF Load)
- Constant Current Sourcing / Sinking Capability using CMOS and Bi-Polar Compound Outputs
- Outputs Swing from Vcc to Vee (Which can be Negative!)
- 3 Amp Peak Source / 5 Amp Peak Sink Current
- Outputs can be Paralleled
- Independent Inputs (TTL Compatible)
- Inputs have a Dedicated Input Reference (IN_REF)
- Fast Propagation Times (20nS typical)
- Shutdown Input Provides Low Power Mode
- Supply Rail Under-voltage Lockout
- Package Options; SOIC-8 & LLP-10 (4x4mm)

Typical Applications

- Sync Rectifier Gate Drivers
- Switchmode Power Supplies
- Solenoid and Motor Drivers
- Power Level Shifter

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The Art of Analog 77

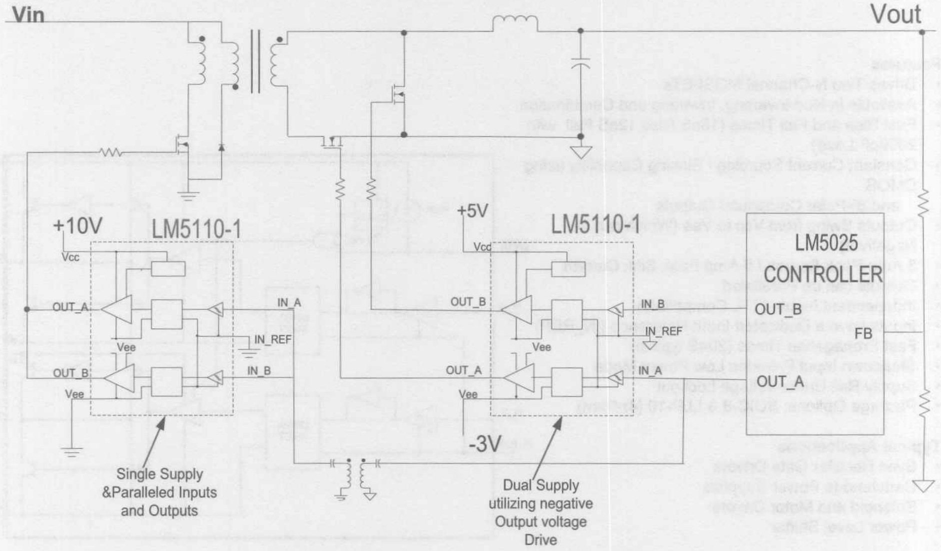
The LM5110 is a versatile and powerful dual gate driver, whose output stage is a "compound " design whereby both MOS and Bipolar devices are placed in parallel. This configuration allows the benefits of the current source characteristic of the Bi-polar devices with the low saturation characteristics of the MOS devices, thereby switching the external gates faster with more drive in the "Miller Region".

Another unique feature of the LM5110 is the built in level shifter. The Vee pin can be negative relative to the IN_REF pin. This allows the user to swing the output both positive for turn-on and the negative for turn-off. This feature can further reduce switching time especially with low threshold voltage FETs. If this feature is not needed, simply connect IN_REF and Vee to the system ground.

The high peak currents necessary for fast switching are available from the drivers which are rated at 3A (source) and 5A (sink).

Since the inputs are TTL-compatible, drive requirements are simple.

LM5110 Gate Driver with Negative Drive Capability



Single Supply
&Paralleled Inputs
and Outputs

Dual Supply
utilizing negative
Output voltage
Drive

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Shown here is an example of how two LM5110 drivers can be used to operate the FET's in a switching converter. The device on the secondary side driving the low threshold voltage sync rectifiers utilizes the level shift feature, with the output swing from 5V (on) to –3V (off). The device on the primary is configured with parallel inputs and outputs for maximum drive current, with the output swing from 10V (on) to 0V (off).

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Portable Power Applications

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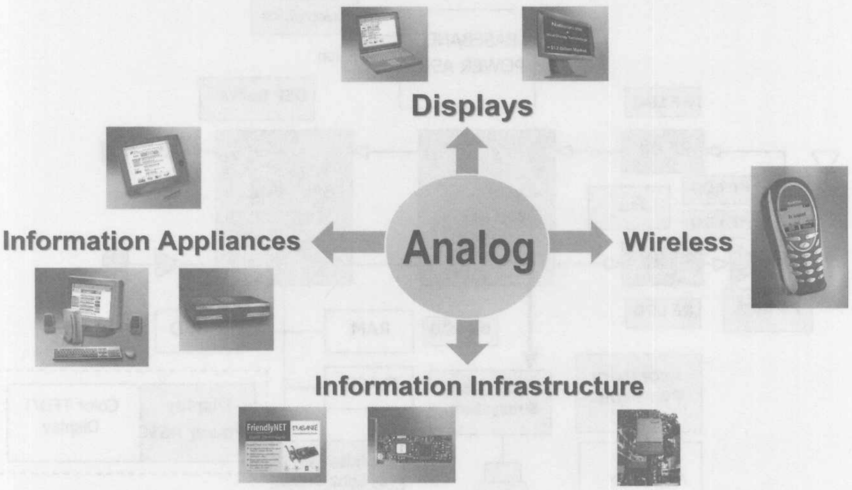
PPS Markets



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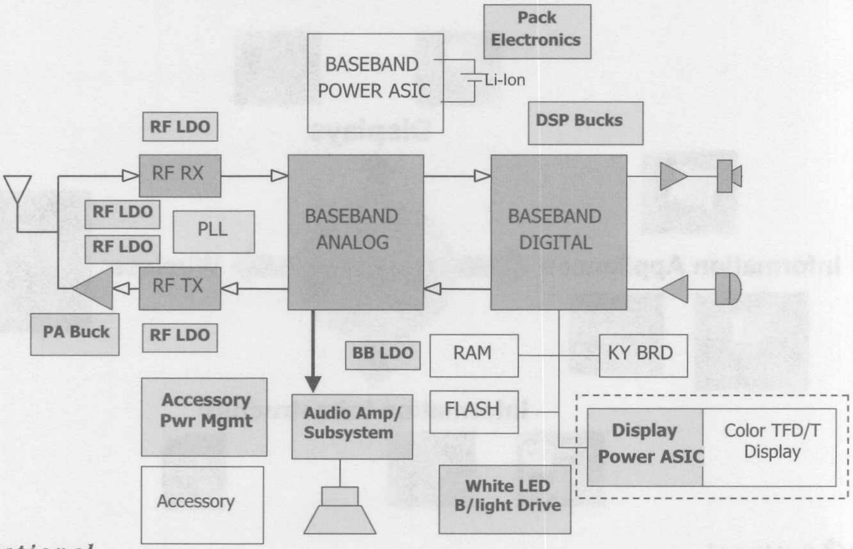
The Art of Analog 3

Analog is the technology at the core of our focus markets
Displays; including:
· LCD, LED, TFT & CRT display circuits (*Liquid Crystal Display, Light Emitting Diode, Thin
· Film transistor, cathode ray tube
· Image and temperature sensors
· Touch-screen technology
Wireless; examples of products in this market are:
GSM, CDMA, DECT (*Global Std for Mobile Communications, Code Division Multiple Access, Digital European Cordless Telecommunications) Bluetooth™
Radio through baseband
All were built on analog solutions such as power management, audio and display driver technology.
Information Infrastructure; including:
· Copper communication
· 3G basestation
Information Appliances; including reference designs for:
· WebPAD™ devices
· Thin-Client terminals
· Set-Top boxes

Building Blocks in Cellular Terminals



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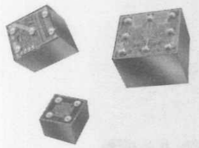
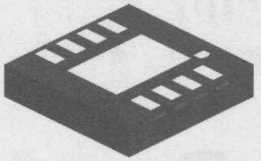
Anticipate market needs to allow fast time-to-market with off-the-shelf high-performance components
Spin variants quickly (3-6 mos.) for specific customer needs
Provide proven circuits for integration
Currently available modules:
LDOs
Charge pumps
Switching regulators
Embedded processors
Boomer / audio amps
Data converters
White-LED drivers
Baseband buck switchers
RF PA switchers
Battery circuits
Audio subsystem / Codec

Chip Scale Packaging



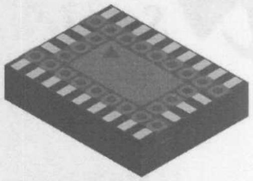
micro SMD

- Application drivers:
  - Mobile handset, PDA, digital camera
- Product drivers:
  - Power, audio, amps, system sensors, etc
  - LP1986 (K45 platform)



Leadless Leadframe Package

- Application drivers:
  - Mobile handset, pcs, network interface
- Product drivers:
  - Power, high power audio, ADC, networks
  - LP2989 (GSM modules)



Laminate CSP / FBGA

- Application drivers:
  - Mobile handset, PCs, network interface
- Product drivers:
  - RF wireless, ADC, networks
  - LMX2379 (P35 platform)

Key requirements for portable applications are

Small size (total solution foot print)

Low cost (total solution cost)

Minimum power consumption (maximum efficiency)

To meet these requirements, National Semiconductor Corp. has developed new processes which yield minimum practical circuit geometries, permitting high performance mixed signal and power devices in small die size.

To enable high power operation in small foot print, new packages such as micro SMD (surface mount devices), LLP (leadless lead frame package) and laminate CSP (chip scale package) FBGA (flex ball grid arrays) have been developed.

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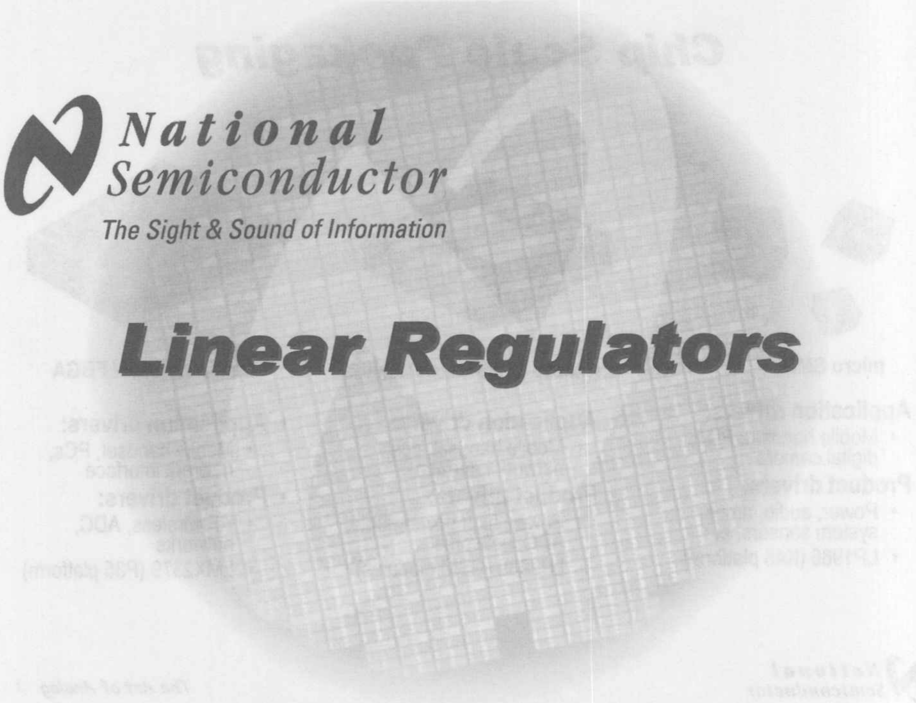
The Sight & Sound of Information



Linear Regulators

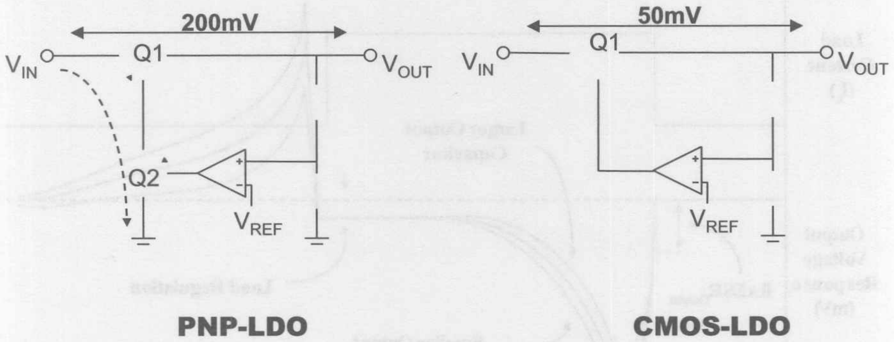
Cmos Linear Regulators

LP3981	300 mA output current
LP3982	Adj LDO with 300 mA output in SOT23
LP3983	Ultra low Iq LDO 5 mA output current
LP3984	150 mA LDO for digital applications
LP3985	150 mA LDO for RF, Analog & general purpose
LP3986	Dual LP3985
LP3987	150 mA LDO with Sleep Mode (14 µA @ 3 mA output)
LP3988	150 mA LDO with Power Good flag
LP3992	25 mA, SOT23, Low Iq
LP3995	Improved LP3985. Active pull-down on output pin
LP3999	LP3995 without active pull-down on output

CMOS LDO Product Family Matrix

	Application	Application				DropOut	Noise	Load	Line	Fast	MicroSMD	Plastic
Product ID	RF/Analog	Digital	Vout <2.5	Iout>50mA	Iq<50µA	<50mV	<30µVrms	Transient	Transient	Turn-On	Package	Package
LP3985	■			■		■	■				■	■
LP3984		■	■	■		■	■	■		■	■	
LP3983		■	■		■						■	
LP3988		■		■		■					■	■
LP3995/9	■		■	■		■	■			■	■	

Bipolar LDO vs. CMOS LDO



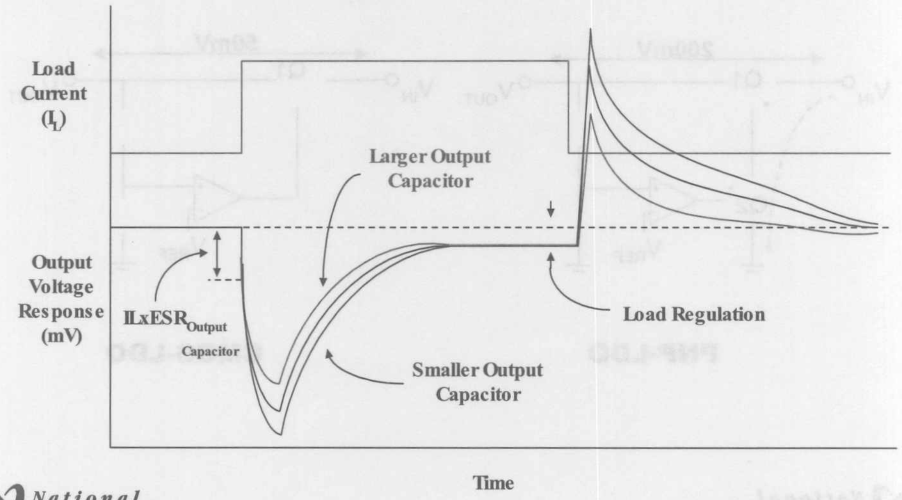
The primary diference between a bipolar LDO and CMOS LDO, aside from the process, is the pass element's mode of operation.

In a bipolar LDO the pass element is a current mode device which means to get more current from its output, more current has to be drained through the base of the pass transistor. There is a practical limit to how much current can be drained through the base of the pass transistor to lower the dropout voltage. Since this current passes through the control circuits and is not part of the current passing through the load, it is considered as waste contributing to inefficiency.

In contrast a CMOS LDO with a MOSFET pass transistor is a voltage-controlled element and acts as a voltage controlled resistance. The pass element's resistance is controlled by the gate voltage and current going through the gate is negligible.

To get lower dropout, the pass transistor has to be made larger to reduce its RDS_{ON}.

Optimizing LDO's Load Transient Response



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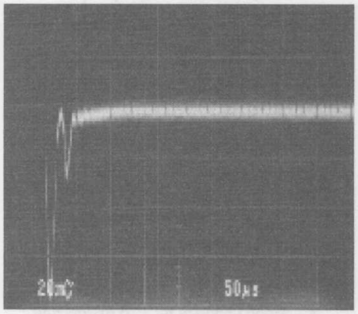
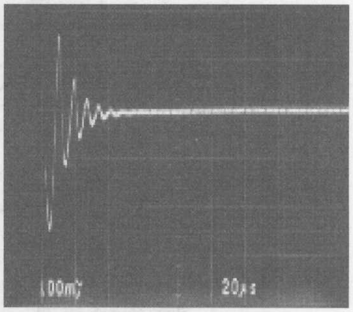
C_{OUT}, the capacitance of the output capacitor, and its ESR are primary factors in stability as well as output dynamic performance.

A large output capacitor tends to provide better load transient response and lower the output noise of the regulator. However, the side effects are potentially slower ON and OFF time and a longer output settling time as indicated on this graph.

Effect of C_{OUT} on Stability (Design Example)



Transient response for load step
Large C_{out}
Still stable, more ringing



Transient response for load step
Small C_{OUT}
Rings heavily, marginally stable

Un-stable operation likely due to improper output capacitor type or value.

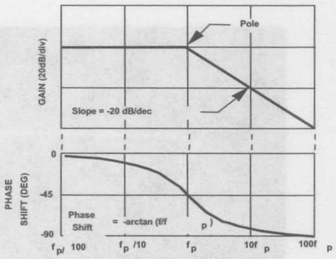


FIGURE 8. POLE GAIN/PHASE PLOT

- Slope changes by -20 dB/decade.
- Phase shift of -90° (max).
- Most of the effect is within one decade (up or down) of f_p.

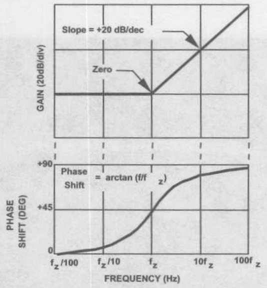


FIGURE 9. ZERO GAIN/PHASE PLOT

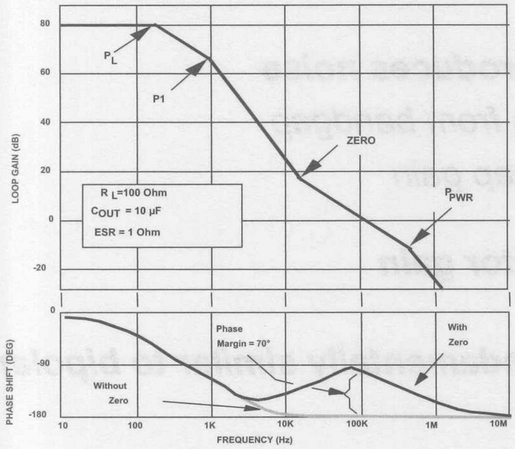
- Slope changes by +20 dB/decade
- Phase shift of +90° (max).
- Acts like an "anti-pole", which means it can cancel out the pole.

To understand the cause and effect of output capacitor value and type, a basic reminder in control loop theory might be helpful.

A pole creates a –20 dB gain rolloff and -90 deg phase shift starting a decade before the pole frequency.

A zero creates a +20 dB gain rolloff and +90 deg phase shift starting a decade before the zero frequency.

Stabilizing the LDO Loop



ESR ZERO STABILIZES LDO

- When the output capacitor ESR is 1 Ohm it adds a zero at 16kHz
- The zero adds about +81° of positive phase shift @ 0 dB.
- The zero brings the total phase shift @ 0 dB back to -110°
- The phase margin is increased to +70° . Loop is stable.

$P_L = 1 / (2p X (R_{LOAD} + R_{ESR}) X C_{OUT})$
P1 = 1kHz (internal)
Zero = $1/(2pR_{ESR} C_{OUT})$
P_{PWR} = PNP or PFET drive

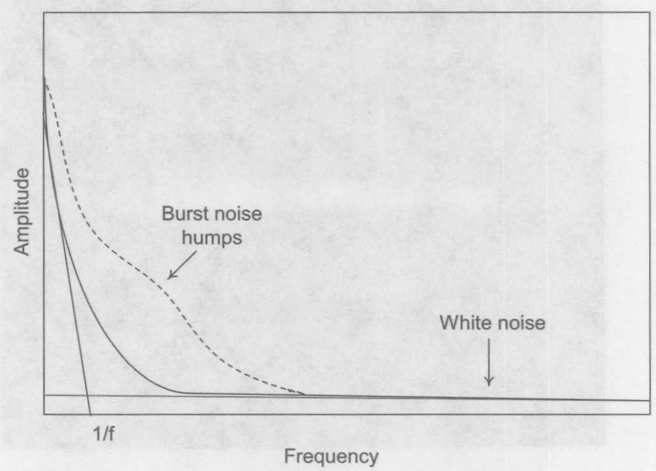
The pole P_L is a product of the load current and the output cap. Any changes made to this pole outside the compensated range by increased load current or incorrect output capacitance value could compromise the phase margin and create an unstable operating condition.

Where Does LDO Noise Come From ?

- *Internal reference produces noise*
  - –Resistor-type noise from bandgap
  - –Amplified by bandgap gain
- *Amplified by regulator gain*
- *CMOS reference fundamentally similar to bipolar*

Many sources could contribute to noise generation in a semiconductor IC. In an LDO, the primary noise source is the bandgap reference. Depending on the type of circuit, the characteristic of the noise would be different. The next slide illustrates the signatures from various noise types.

Noise in Frequency Domain



Covering noise in detail is beyond the scope of this seminar but we will make an attempt to briefly cover the highlights.

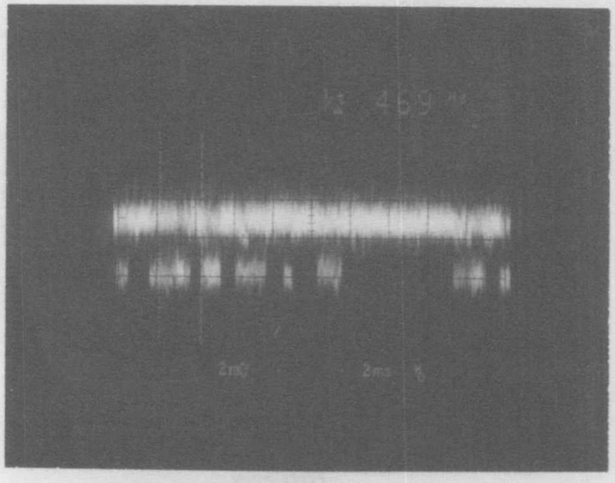
This is an illustration of various noise signatures in the frequency domain.

The white noise is generated by the resistive elements in the circuits. Its frequency spectrum covers a very wide frequency range. The white noise amplitude, which is a function of the resistor value, is fairly constant over the frequency range.

The burst noise generally shows up below 10 kHz and 1/f noise is mostly around 100 Hz or so.

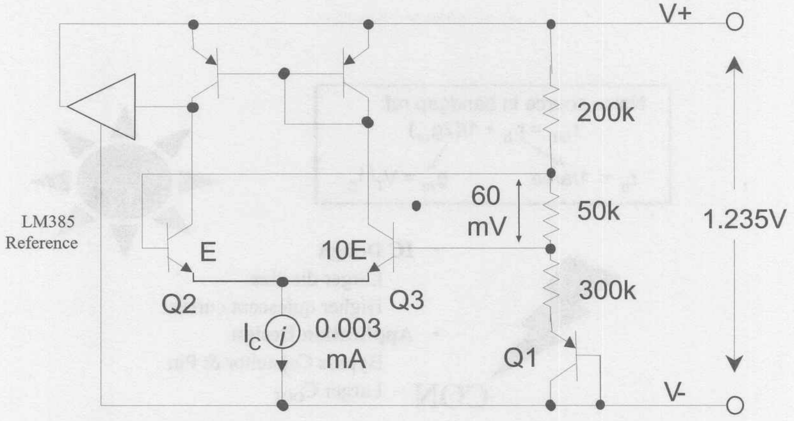
A scope photo of the 1/f noise is illustrated on the following slide.

An Example of a Classic Popcorn Noise



This is a historic photo. You will have to try really hard to come up with noisy circuit like this (of course this picture is of a competitors part).
The 1/f noise shown here in a time domain display (scope photo) appears like a serial digital code switching hi and low, but the amplitude is in mV.

Bandgap Reference



$[V_{BE\,(1E)} - V_{BE\,(10E)}]$ x10 =600mV + 2mV/deg C

Diode =600mV - 2mV/deg C

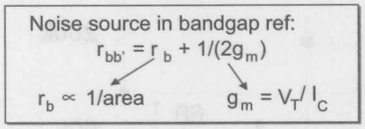
1.2V with no Tempco @ 25 deg C

A simplified bandgap circuit is illustrated here. Operation of the circuit is illustrated by the formula on the slide.

Q3 is 10 times larger than Q2 in geometry thus generating a 60 mV Vbe mismatch at 25° C. This voltage is temperature dependent and will change by + 2mV/° C (thus called PTAT, Proportional To Absolute Temperature). Pairing this voltage with diode Q1 with opposite thermal characteristic will produce a temperature-independent 1.2V source which is used in LDOs as a voltage reference.

As we will see on the next slide, the physical size of the Q2 and Q3 and the magnitude of the IC current determines the output noise of the band gap and thus the LDO.

Noise Tradeoffs


Noise source in bandgap ref:

$r_{bb'} = r_b + 1/(2g_m)$

$r_b \propto 1/\text{area}$

$g_m = V_T / I_C$

PRO

CON

- **IC Design**
  - Larger die size
  - Higher quiescent current
- **Application Design**
  - Bypass Capacitor & Pin
  - Larger C_{OUT}

As indicated here, increasing the area or the size of Q2 and Q3 or increasing the current through the transistors will reduce the noise, but do we really want this ?

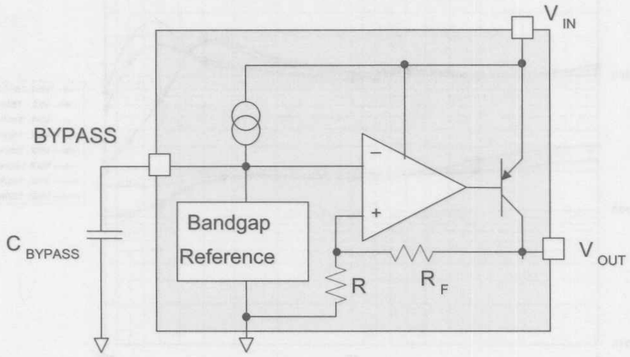
Larger die size ? This is a cardinal sin but nobody wants to do this unless he/she rrreeeeaaallllyy wants low noise or doesn't care about die size, but in portable applications we do.

Increasing the current through the bandgap core is equally sinful and goes against the drive for efficiency.

But there are solutions out there, we will explore these solutions on the following slides.

Typical Bypass on Reference Output

Plusses	***Minuses***
• **Reduces noise by 5-10x**	• **Requires extra pin & capacitor**

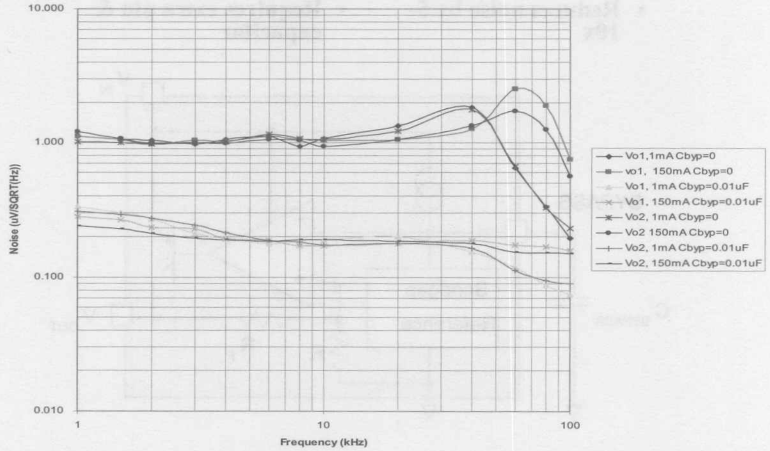


This is a block diagram for a typical bipolar LDO. A CMOS LDO will have a fairly similar simplified diagram.

The simplest solution is to add a capacitor between the output of the bandgap reference to ground to create a low pass filter.

As with most engineering solutions, nothing is free and there are trade off's.

Output Noise Spectral Density

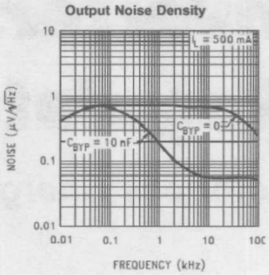


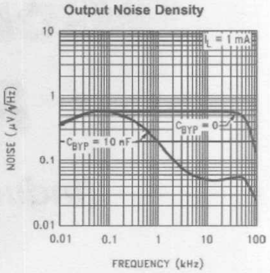
The effect of a noise bypass capacitor is illustrated here in frequency domain.

Noise Specifications in Low-Dropout Regulators

Symbol	Parameter	Conditions	Typical	LP2989AI-X.X (Note 6)		LP2989I-X.X (Note 6)		Units
				Min	Max	Min	Max	
e_n	Output Noise Voltage (RMS)	BW = 100 Hz to 100 kHz, C_{OUT} = 10 µF C_{BYPASS} = .01 µF V_{OUT} = 2.5V	18					µV(RMS)

Noise density shown in typical performance curves


Output Noise Density


Output Noise Density

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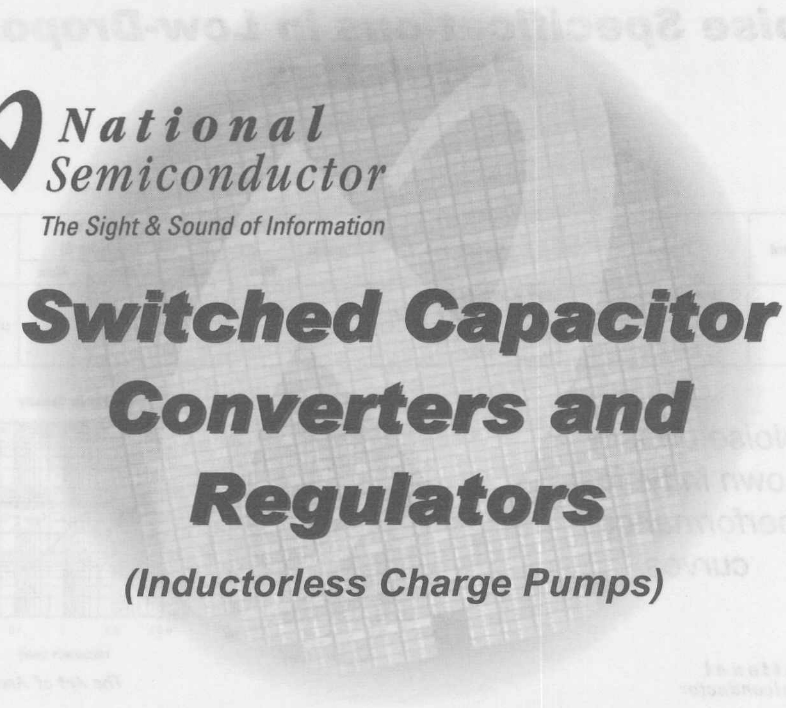
Device	Max. Load	RMS Noise	Test Bandwidth	Conditions
LP2989	500 mA	18 uV	100 Hz ~ 100 kHz	V_{OUT}=2.5V, C_{OUT}=10uF, C_{BYP}=10nF
LP2992	250 mA	30 uV	300 Hz ~ 50 kHz	V_{OUT}=3.3V, C_{OUT}=10uF, C_{BYP}=10nF
LP2988	200 mA	20 uV	300 Hz ~ 50 kHz	V_{OUT}=3.3V, C_{OUT}=10uF, C_{BYP}=10nF
LP3985	150 mA	30 uV	10 Hz ~ 100 kHz	V_{OUT}=3.3V, C_{OUT}=1uF, C_{BYP}=10nF
LP2985	150 mA	30 uV	300 Hz ~ 50 kHz	V_{OUT}=3.3V, C_{OUT}=10nF, C_{BYP}=10nF



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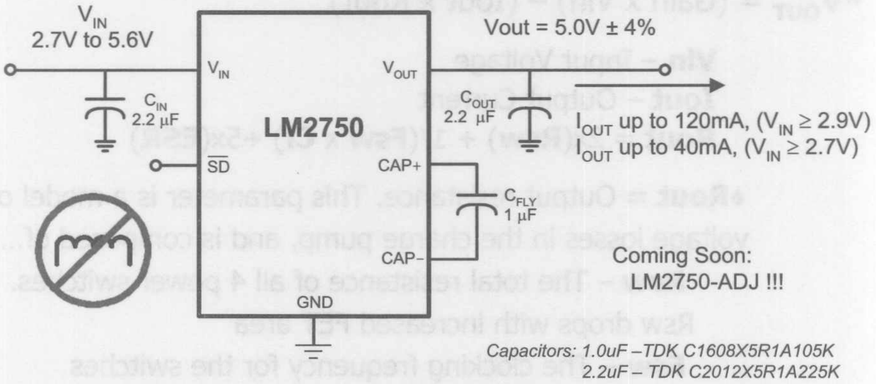
The Sight & Sound of Information

Switched Capacitor Converters and Regulators

(Inductorless Charge Pumps)

A different class of regulators offering better efficiency, are switched capacitor converters.

LM2750: Li-Ion to 5V Converter



Vout = 5.0V ± 4%

I_{OUT} up to 120mA, ($V_{IN} \geq 2.9V$)
I_{OUT} up to 40mA, ($V_{IN} \geq 2.7V$)

Coming Soon:
LM2750-ADJ !!!

Capacitors: 1.0uF – TDK C1608X5R1A105K
2.2uF – TDK C2012X5R1A225K

Regulated switched capacitor doubler (2×)
no inductor!!

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Application circuits are very simple and generally require an additional capacitor other than the input and the output capacitors. A typical switched-capacitor circuit is shown here.

Basic Charge Pump Conversion Equation

- **V_{OUT}** = (Gain x Vin) – (Iout x Rout)

Vin – Input Voltage
Iout – Output Current
Rout = 2x(**Rsw**) + 1/(**Fsw** x **Cf**) +5x(**ESR**)

♦**Rout =** Output resistance. This parameter is a model of voltage losses in the charge pump, and is composed of…

Rsw – The total resistance of all 4 power switches. Rsw drops with increased FET area
Fsw – The clocking frequency for the switches
ESR – The capacitor internal resistance
Cf – The flying capacitor

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As stated above, output resistance (Rout) is a model of all internal voltage losses in the charge pump … it is not a "real" resistor. Since the magnitude of these losses are proportional to the output current of the charge pump, the losses are commonly simplified to the "Rout" parameter.

Regulating V_{OUT}

- V_{OUT} = (Gain x Vin) – (Iout x Rout)
  - Possible Regulation Schemes:
    - Regulate **Gain**?
      - Too many gain choices for SwCap – Not Practical
      - Can provide benefits for Efficiency
    - Post-Regulation
      - SwCap Doubler Followed by a Linear Regulator (LDO)
    - Regulate **Rout**
      - **Rout** = 2x(**Rsw**) + 1/(**Fsw** x **Cf**) +5x(**ESR**)
      - Control **Fsw**:
        - Pulse-Frequency Modulation (PFM)
      - Control **Rsw**:
        - Pre-Regulation **(choice for LM2750)**

Example of gain regulation: Pulse-width modulated inductive switch-mode regulators regulate Vout by adjusting the gain of the conversion. This is done by modulating the duty cycle of the switching ON/OFF times. Since duty cycle can be modulated continuously, a PWM-type inductive regulator can optimize gain as conditions vary (input voltage variations, output current variations, etc.).

A gain-modulation scheme is not possible with switched capacitor regulators, and is the reason why inductive regulators are much more efficient than switched capacitor regulators when running off a variable input voltage source, such as a Li-Ion battery.

The extra efficiency of an inductive-based regulator comes at a heavy price, however, when the additional solution size, cost, and noise of the inductor are factored in.

Design for Minimum Rout

Vout = 2xVin – (Iout x Rout)

Constraint on **Rout**: Must be low enough to ensure the part remains in regulation under worst case conditions. LM2750 example:

- *Minimum Vin (Vin = 2.9V)*
- *Maximum Iout (Iout = 120mA)*

Constraint: Rout ≤ 6.67 Ohms

Rout = 2x(**Rsw**) + 1/(**Fsw** x **Cf**) +5x(**ESR**)

Rsw = ?
Fsw = 1.7MHz
Cf = 1uF
ESR = 0.01 Ohm

Switch Size Constraint: Rsw ≤ 3 Ohms !!

In this LM2750 example, the switches need to be sized for the worst case:
Vin = 2.9V, Iout =120 mA.
Big switches are required to get such a small switch impedance.
Switches take up the majority of the die size in charge pump ICs, and thus are often directly proportional to the cost of a device.

Output Ripple

Vripple = **Iload**/2(**Fsw** x **Ch**) + 2(**Iload** x **ESR**)

- **Fsw** – The clocking frequency for the switches
- **ESR** – The capacitor internal resistance
- **Ch** – The hold capacitor at Vout (ex: use 1uF)
- **Worst Case** at maximum load (120mA)

Fsw = 170kHz:

Vripple = 120mA/2(170k x 1u) + (120mA x 0.02)
= **355mV**

Fsw = 1.7MHz:

Vripple = 120mA/2(1.7M x 1u) + (120mA x 0.02)
= **38mV !!**

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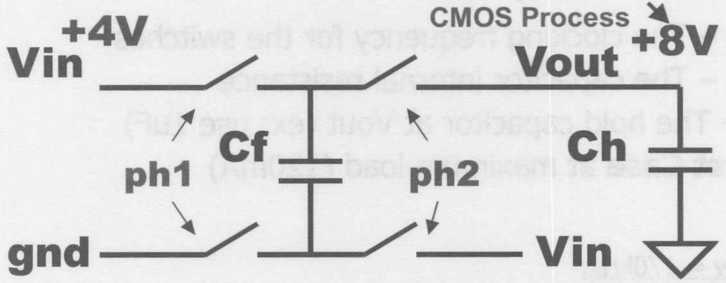
Increasing Clock Frequency by 10X yields almost 10X improvement in Output Ripple!
Larger hold Cap (Ch) can further improve Vripple.
Fixed switching frequency > 1MHz is often beneficial in phone designs, as it minimizes the risk/possibility of noise interfering with other phone functions.

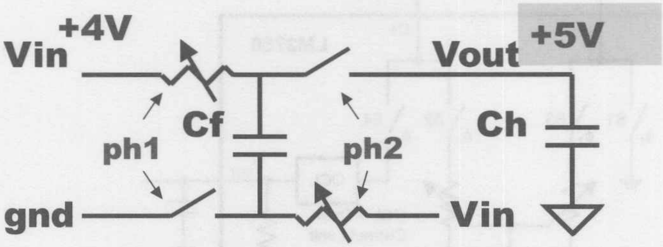


Too High for Fine Line CMOS Process

Four power FET switches clocked in pairs

A normal Switched Cap Doubler (unregulated) creates Vout = 2 x Vin.
Charge the flying cap (Cf) in phase 1 to Vin.
Stack Cf on Vin in phase 2 to get: Vout = 2 x Vin.

LM2750 Switching



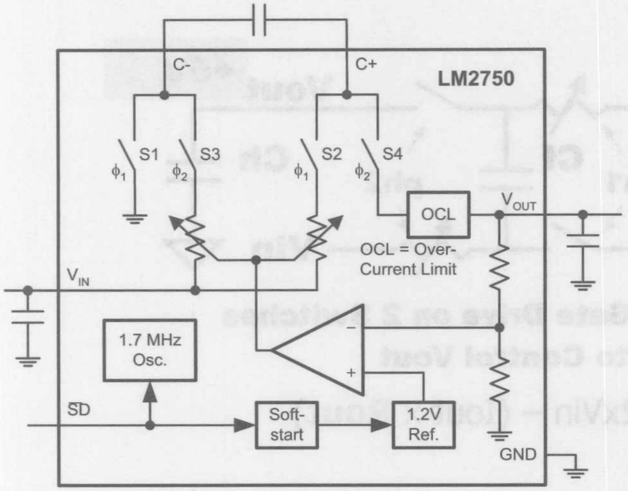
Regulate Gate Drive on 2 Switches to Control Vout

$$V_{out} = 2 \times V_{in} - (I_{out} \times R_{out})$$

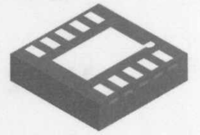
Switching is done the same way as normal 2x pump.
Now we regulate the gate drive on 2 switches to control Rout.
In phase 1 we may not charge the cap all the way to Vin.
In phase 2 we may not stack the cap on a full Vin.
Regulation is designed to yield Vout = 5V.

LM2750: Li-Ion to 5V Converter

Block diagram



LLP-10 Package



3mm × 3mm × 0.8mm

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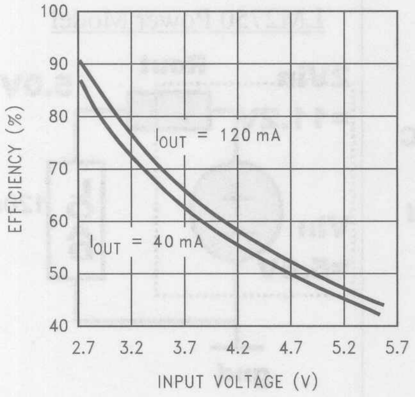
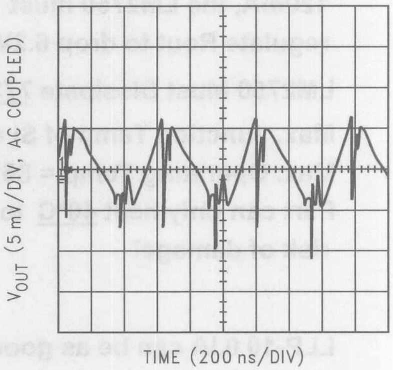
LM2750: Li-Ion to 5V Converter

Power efficiency



Output ripple



I_{OUT} = 120 mA

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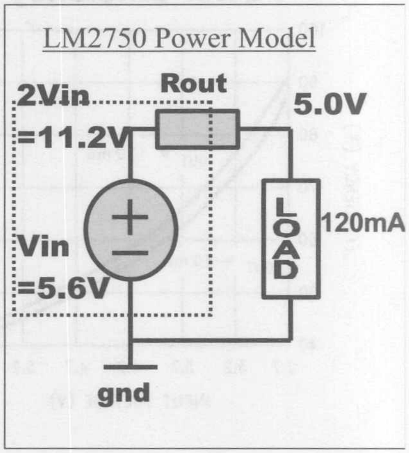
Power Dissipation in LM2750

At High Vin = 5.6V and Iload = 120mA, the LM2750 must regulate Rout to drop 6.2V.

LM2750 Must Dissipate <u>773mW</u>

Max. Junction Temp of Si =125°C
Max. Operating Temp = 85°C
Part can only heat <u>40*C</u> to avoid risk of damage!

LLP-10 θJA can be as good as 50°C / W with good board layout

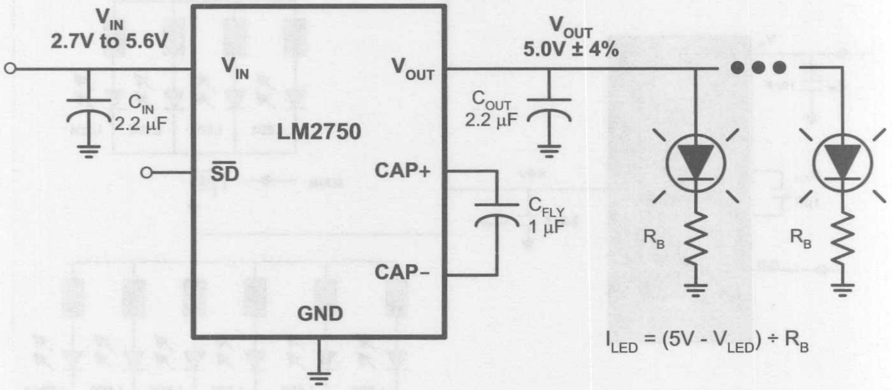


Power Dissipated (Pd) = Power In (Pin) – Power Out (Pout).
Pd = [Vin x (2xIout + Iq)] – [Vout x Iout]
Pd(max) = [5.6 x (2x.120 + .005)] – [5 x .120]
= 0.773 W

θJA (qJA) is a package characteristic that describes how much the temperature in the package will rise with the power dissipated in it. θJA for a given package is greatly affected by the pcb layout and other considerations for dissipating heat from the package.

Temperature Rise = θJA x Power-Dissipated

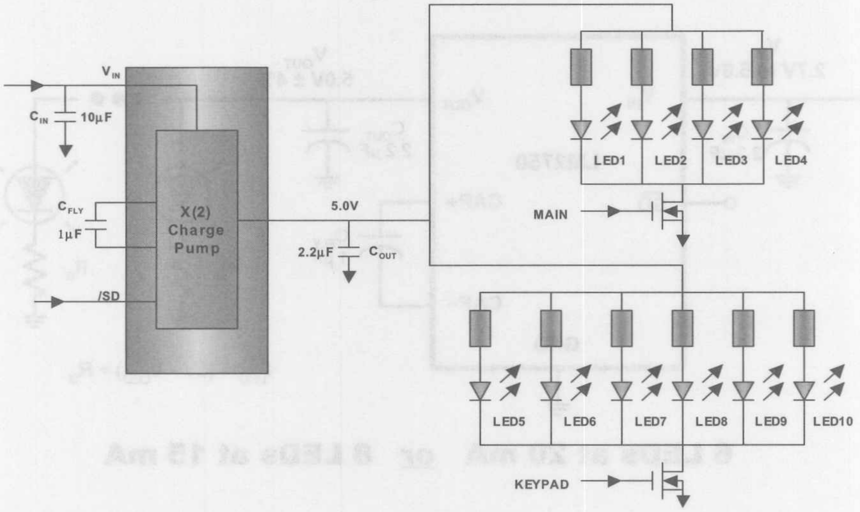
LM2750 Drives White-LEDs



$I_{LED} = (5V - V_{LED}) \div R_B$

6 LEDs at 20 mA *or* **8 LEDs at 15 mA**

Regulated SWCAP LED



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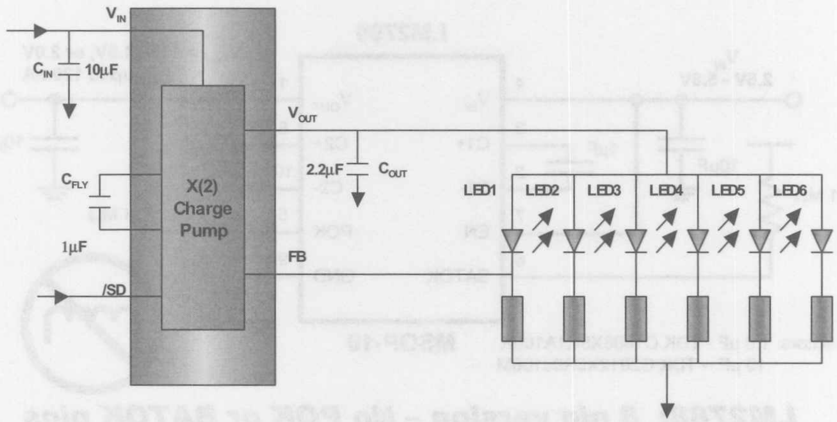
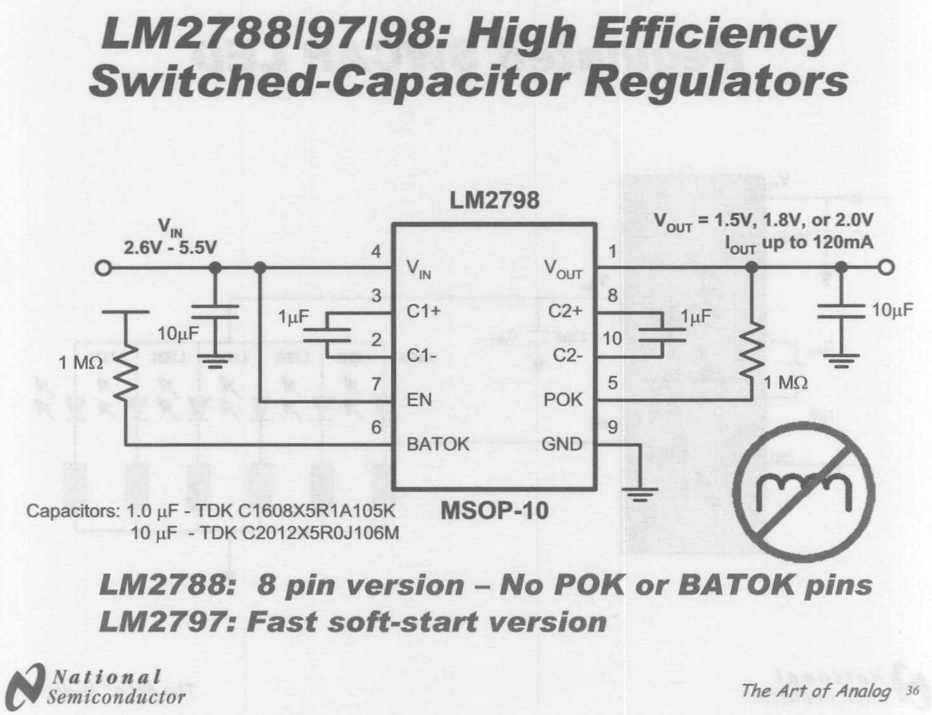
The Art of Analog 34

Feature	Benefit
2x charge pump	Boost Li-ion battery to drive white/blue LEDs.
SD	Save power during sleep mode.
High switching frequency of 1.7 MHz	Low output voltage ripple (+/- 5mV peak-peak).
Regulated voltage	Drives LEDs at a constant brightness.
Low input noise with a pre-regulation loop	Limits conducted noise to the system. Reduces possibility of RF interference due to switching noise.
Small LLP 10 pin package 3 mm x 3 mm x 0.8 mm	Same size as a SOT23-5 footprint. Low device height makes thin form factor possible.

Regulated SWCAP LED





LM2788/97/98: High Efficiency Switched-Capacitor Regulators

Capacitors: 1.0 µF - TDK C1608X5R1A105K
10 µF - TDK C2012X5R0J106M

LM2788: 8 pin version – No POK or BATOK pins
LM2797: Fast soft-start version

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The Art of Analog 36

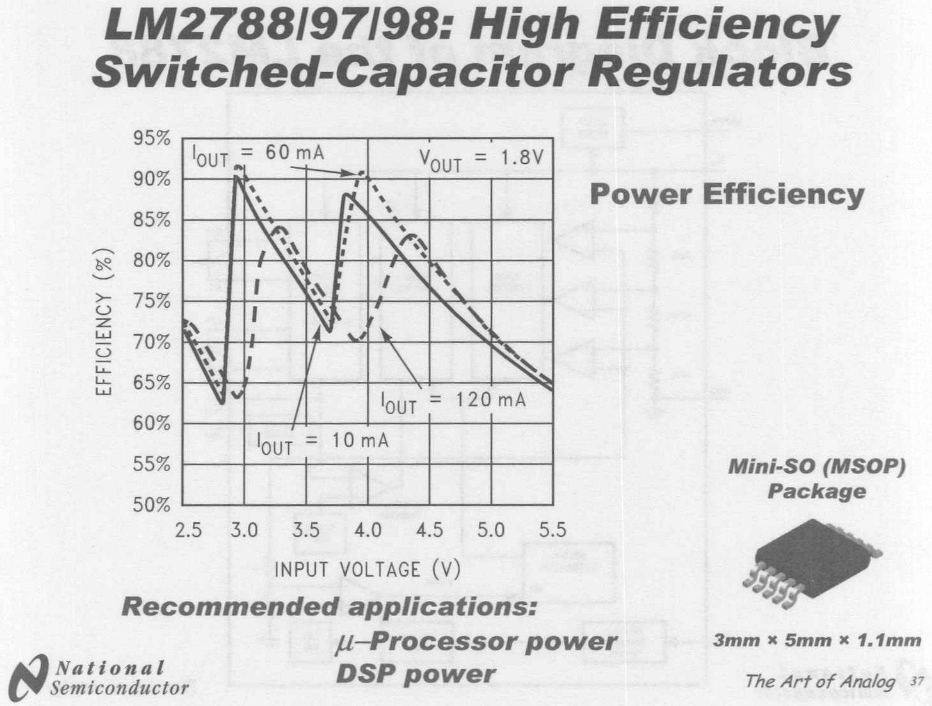
The LM2788/97/98 is a switched capacitor step-down DC/DC converter it efficiently produces a 120 mA regulated low-voltage rail from a 2.6V to 5.5V input. Fixed output voltage options of 1.5V, 1.8V, and 2.0V are available. These parts use multiple fractional gain configurations to maximize conversion efficiency over the entire input voltage and output current ranges. Also contributing to high overall efficiency is the extremely low supply current: 32 mA operating unloaded and 0.1 mA in shutdown.

The optimal external component requirements of the LM2788/97/98 solution minimize size and cost, making them ideal for Li-Ion and other battery powered designs. Two 1 uF flying capacitors and two 10 uF bypass capacitors are all that is required, and no inductors are needed.

The LM2788/97/98 also feature noise-reducing soft-start circuitry (400us turn-on time for LM2788 and LM2798, 100us turn-on time for LM2797), short-circuit protection and over-temperature protection. The LM2797 have input and output voltage monitoring (BATOK and POK)

Features:

- Output voltage options: 2.0V ± 5%, 1.8V ± 5%, 1.5V ± 6%
- 120mA output current capability
- Multi-Gain and Gain Hopping for Highest Possible Efficiency
- 2.6V to 5.5V input range
- Low operating supply current: 32 µA
- Shutdown supply: 0.1 µA
- Thermal and short circuit protection
- Available in an 8-Pin MSOP Package



LM2788/97/98: High Efficiency Switched-Capacitor Regulators

Power Efficiency

Mini-SO (MSOP)
Package

3mm × 5mm × 1.1mm

Recommended applications:

μ–Processor power
DSP power

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The Art of Analog 37

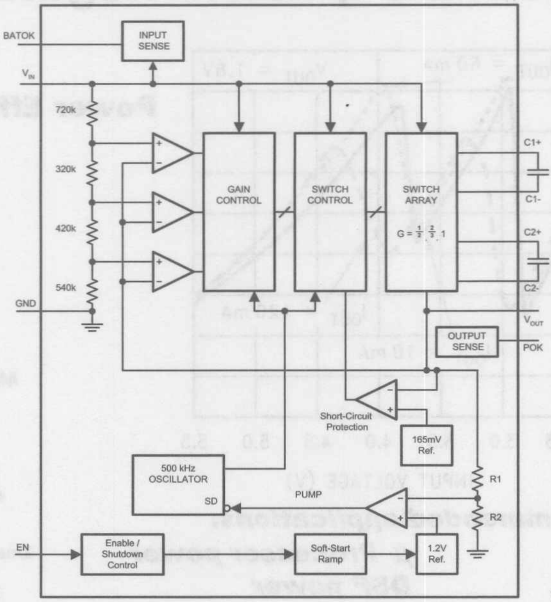
The curve above highlights the efficiency of the LM2788/97/98. The parts use multi-gain switched-capacitor technology to optimize efficiency over the entire input voltage range and output current range. This topology is much more efficient than a linear regulator. It is less efficient than a typical inductive-based switch mode regulator. The drawbacks of an inductor (cost, size, EMI) often make this switched capacitor solution a very attractive middle ground: providing …

•Low cost

•Good efficiency

•Small solution size

Block Diagram of the LM2788



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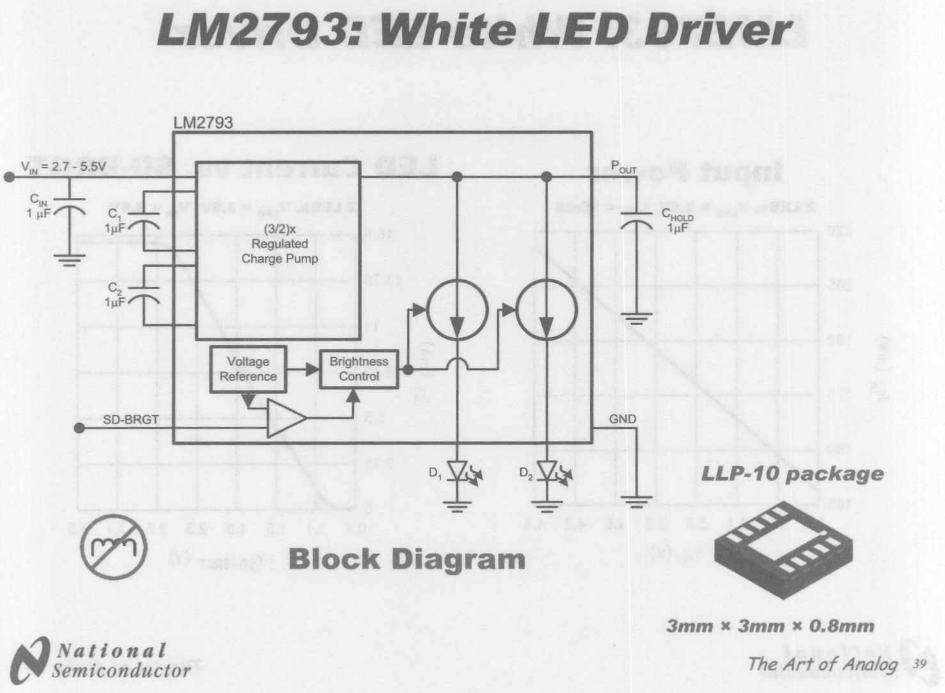
The figure above is the block diagram of the LM2788.

The part operates with a gain of 1/2, 2/3, or 1. The part will operate in the gain configuration that keeps the output voltage regulated at optimal efficiency.

The optimal gain configuration is determined by monitoring the input voltage and output voltage. The gain stages are implemented in the switch array. The switch array uses MOS switches to connect the flying capacitors (C1, C2) either to Vin, Vout, or to each other in the two phases of the charge pump operation.

Block diagrams of the LM2797 and LM2798 are similar, with the additions of input and output voltage monitoring and flag outputs being the only difference.



LM2793: White LED Driver

Block Diagram

LLP-10 package

3mm × 3mm × 0.8mm

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The Art of Analog 39

The LM2793 is a highly-efficient, semi-regulated 1.5x CMOS charge pump that provides dual constant-current outputs. The LM2793 has an input voltage range of 2.7V to 5.5V.

To control LED brightness, the amount of current driven to the current-mode outputs can be adjusted with an analog voltage and/or a pulse-width-modulated (PWM) square wave.

Pre-regulation of the charge pump minimizes conducted noise on the input. Combined with a fixed switching frequency of 500 kHz, the LM2793 is a low-noise solution.

The LM2793 is available in a 10-pin leadless Lead-frame package: LLP-10.

Features:

Two regulated current outputs, up to 16 mA each, matched to within ±0.3% (typ.)

High efficiency, 1.5x regulated charge pump

Input voltage range: 2.7V to 5.5V

Soft start limits inrush current

Analog voltage brightness control

PWM brightness control

Very small solution size - NO INDUCTOR

500 kHz Switching Frequency

3 µA (typ.) Shutdown Current

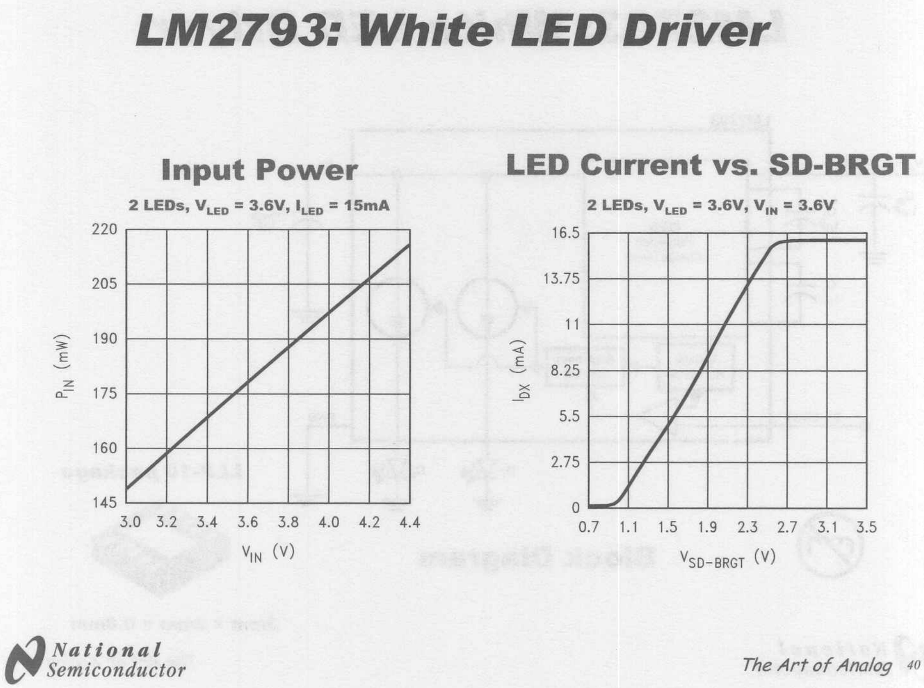
LLP-10 package: 3.0mm X 3.0mm X 0.8mm

Applications:

White LED display backlights

White LED keypad backlights

1-cell li-ion battery-operated equipment including PDAs, hand-held PCs, cellular phones



LM2793: White LED Driver

Input Power

2 LEDs, V_{LED} = 3.6V, I_{LED} = 15mA

LED Current vs. SD-BRGT

2 LEDs, V_{LED} = 3.6V, V_{IN} = 3.6V

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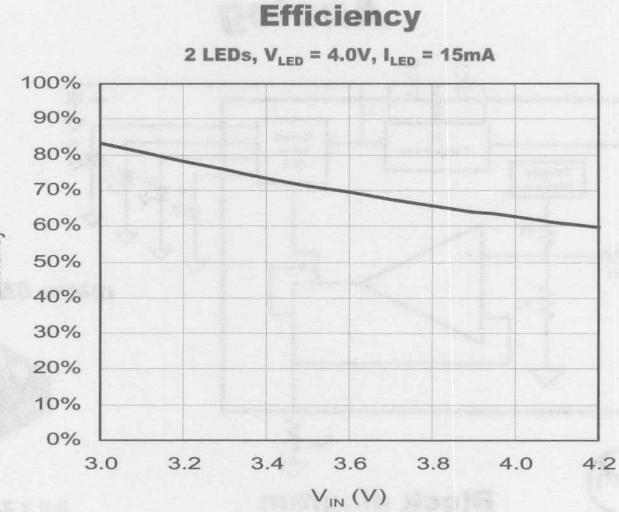
The Input Power graph above shows the power consumption of the typical LM2793 application circuit. Efficiency, as defined as Eff = (Pled / Pin), is in part dependent on LED forward voltage. However, variation in LED voltage does not affect power consumed by the circuit and typically does not relate to the brightness of the LED for constant current LED drivers . It is recommended that power consumed by the circuit be evaluated instead.

SHUTDOWN AND BRIGHTNESS CONTROL

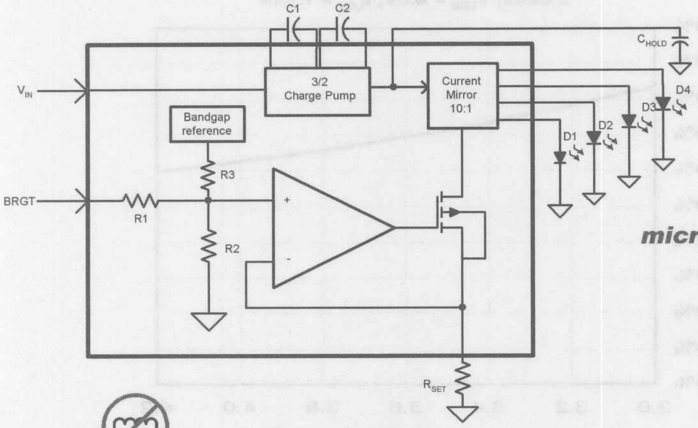
The LM2793 has an active-low, dual function shutdown/brightness control pin, SD-BRGT. A voltage higher than 0.65V (typ) on SD-BRGT will put the LM2793 in active mode. Applying a voltage below 0.35V (typ) on the SD-BRGT pin will turn off the device, reducing the quiescent current to 3µA (typ).

The LM2793 has the ability to adjust LED brightness by applying an analog voltage or a PWM signal to the SD-BRGT pin.

LM2793: White LED Driver

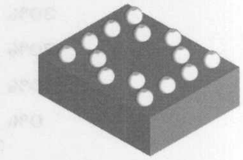


LM2794/95 – Current Regulated Switched Capacitor LED Supply with Analog



Block diagram

micro SMD package



2.0 x 2.4 x 0.85 mm body size

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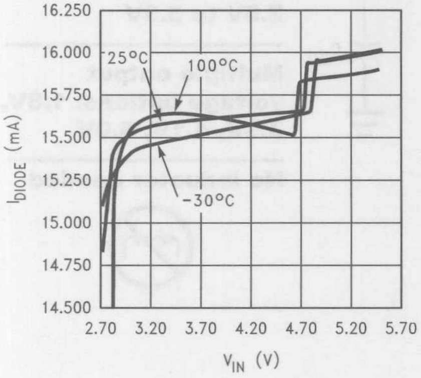
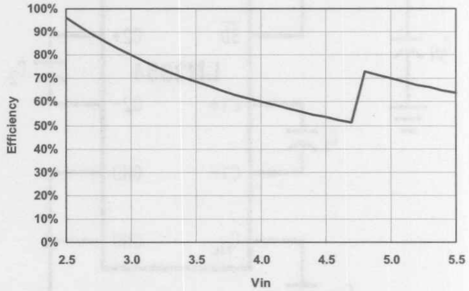
The LM2794/95 is a fractional CMOS charge-pump that provides four regulated current sources. It accepts an input voltage range from 2.7V to 5.5V and maintains a constant current determined by an external sense resistor.

- Regulated current sources with ±0.5% matching between any two outputs
- High efficiency 3/2 boost function
- Drives one, two, three or four white LEDs
- 2.7V to 5.5V Input Voltage
- Up to 80 mA output current
- Analog brightness control
- Active-low or high shutdown input ('94/95)
- Very small solution size and no inductor
- 2.3µA (typ.) shutdown current
- 325kHz switching frequency (min.)
- Constant Frequency generates predictable noise spectrum
- Standard micro SMD-14 package: 2.08 mm X 2.403 mm X 0.845 mm High
- Thin micro SMD-14 package: 2.08 mm X 2.403 mm X 0.600 mm High

LM2794/95 Performance Curves



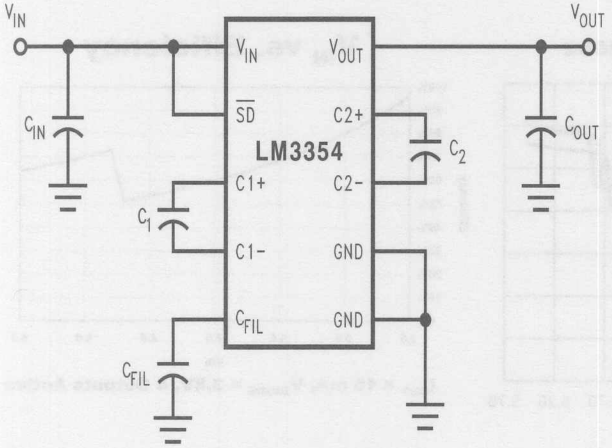
V_{IN} vs. I_{DIODE}



V_{IN} vs. Efficiency

I_{OUT} = 15 mA, V_{DIODE} = 3.8V, 4 Outputs Active

LM3354 Regulated 90mA Buck-Boost Switched Capacitor DC/DC Converter



Input voltage range: 2.5V to 5.5V

Multiple output voltage options: 1.8V, 3.3V, 4.1V, 5.0V

No inductor needed

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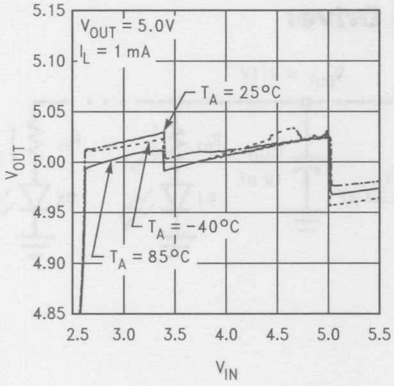
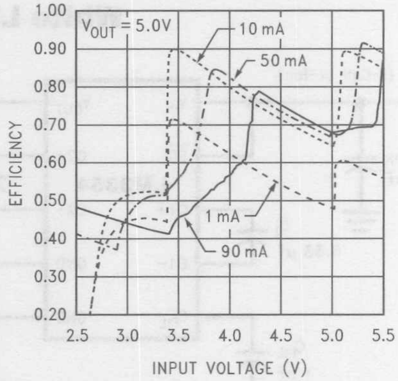
The LM3354 is a CMOS switched capacitor DC/DC converter that produces a regulated output voltage by automatically stepping up (boost) or stepping down (buck) the input voltage. It accepts an input voltage between 2.5V and 5.5V. The LM3354 is available with standard output voltages of 1.8V, 3.3V, 4.1V (ideal for white LED applications), and 5.0V.

- Regulated VOUT with ±3% (5.0V, 4.1V, and 3.3V options) or ±4% (1.8V option) accuracy
- Standard output voltages of 1.8V, 3.3V, 4.1V, and 5.0V
- Custom output voltages available from 1.8V to 5.0V in 100 mV increments with volume order
- 2.5V to 5.5V input voltage range
- Up to 90mA (5.0V, 4.1V, and 1.8V options) or 70mA (3.3V option) output current
- >75% average efficiency
- Uses few, low-cost external components
- Very small solution size
- 375 µA typical operating current
- 2.3 µA typical shutdown current
- 1 MHz typical switching frequency
- Architecture and control methods provide high load current and good efficiency
- MSOP-10 package
- Over-temperature protection

LM3354 Performance Curves



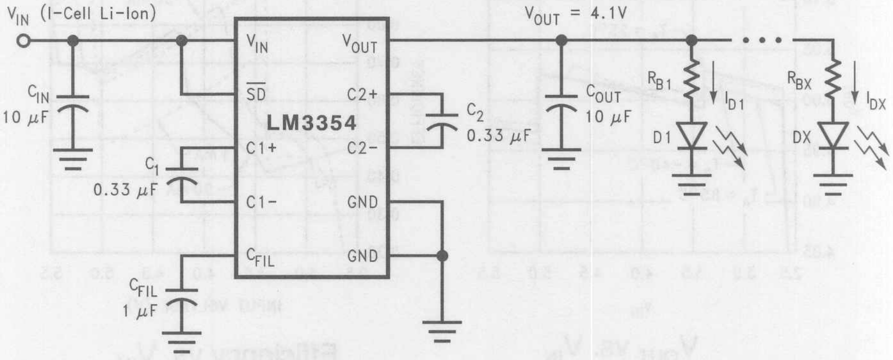
V_{OUT} vs. V_{IN}



Efficiency vs. V_{IN}

LM3354 Applications

White LED Driver



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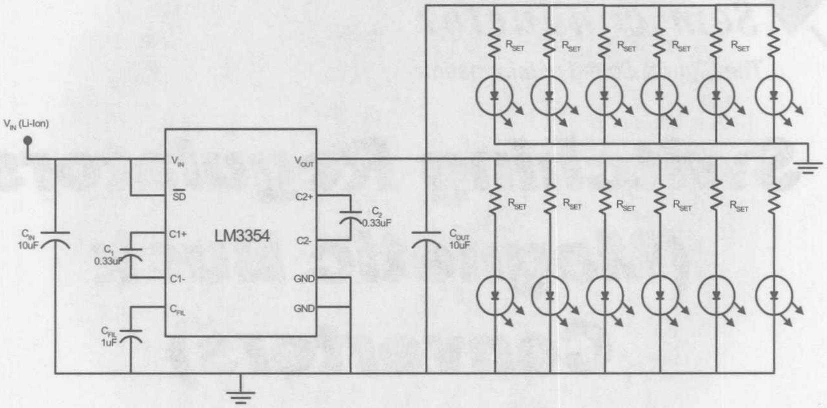
Achieves buck-boost operation without an inductor.
No stability concerns as there are in PWM magnetic buck-boost switchers.
High efficiency achieved with multiple gains and pulse skipping.
Requires only small capacitors eliminating the need for an inductor and its associated cost and EMI.
Can be used in any standard buck, or boost, and buck-boost application or can drive any color LEDs.

LM3354: Typical White LED Backlight for a Phone Keypad.



LM3354-4.1: Drives 12 white LEDs for keypad backlight. Provides high efficiency and high current. LED current is 5mA each. For a 3.6V LED, R_{SET} is 100ohms.

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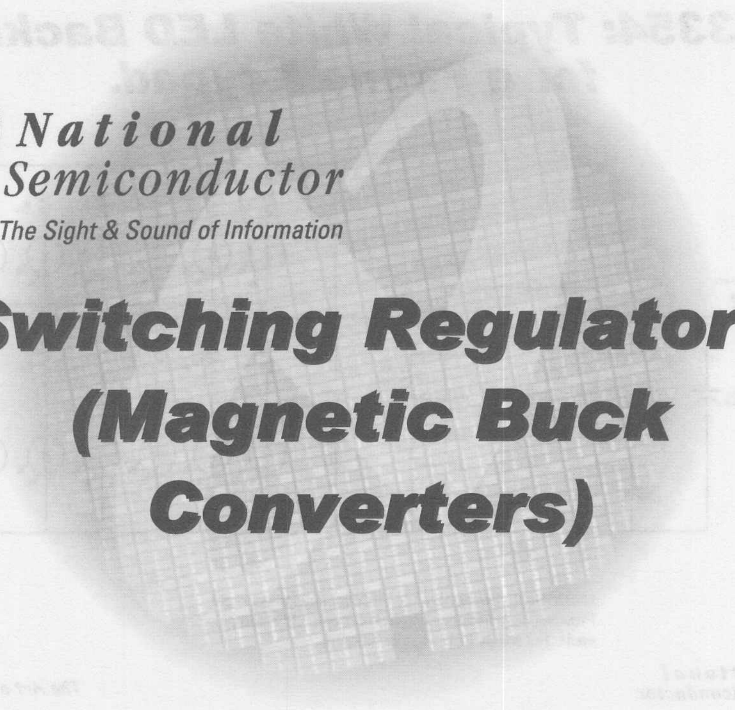
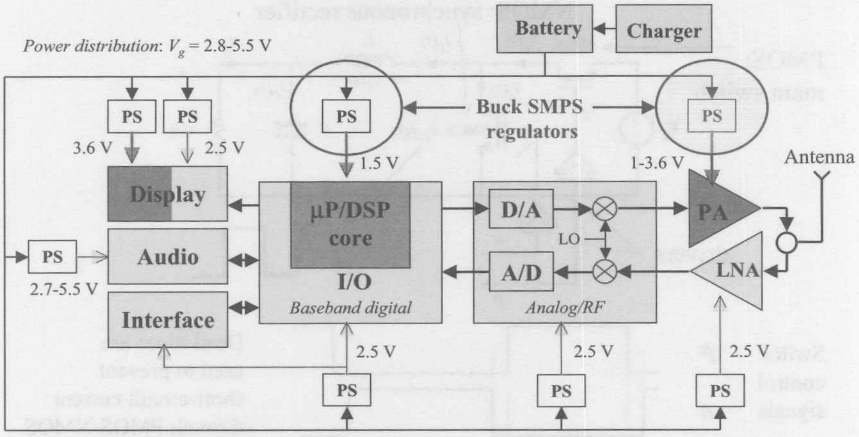


Switching Regulators (Magnetic Buck Converters)

Buck regulators in the system

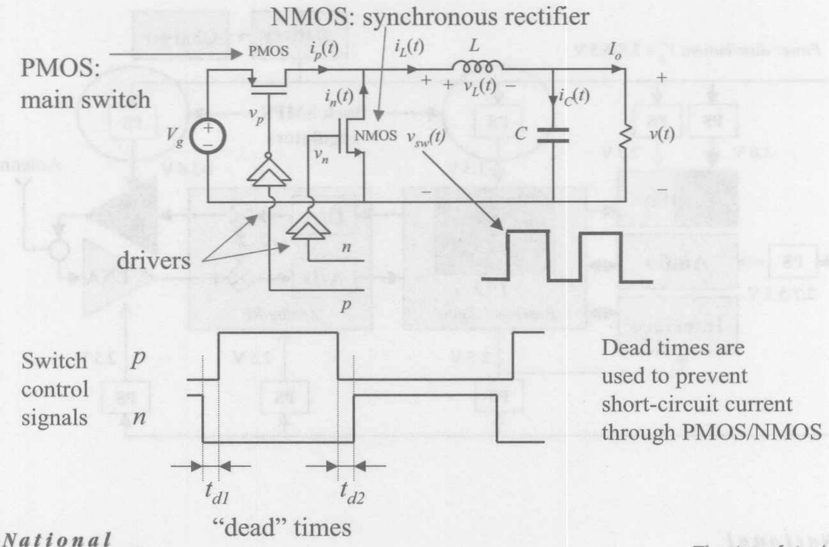


Buck regulators are often used as switch-mode power supplies for baseband digital core and the RF power amplifier (PA)

Selection Guide

Buck Converters	Output Voltages	Output Current	Shutdown Current	Quiescent Current	MODES
LM2608-1.3 ATL	1.3V, 1.5V	300mA/3mA	0.02µA	590µA/20µA	PWM/LDO
LM2608-1.8 ATL	1.5V, 1.8V	400mA/3mA	0.02µA	590µA/20µA	PWM/LDO
LM2612 BL/TL	1.05V, 1.3V 1.5V, 1.8V	400mA/100mA	0.02µA	605µA/160µA	PWM/PFM
LM2614 ATL	1.0V – 3.6V (Adjustable)	400mA/100mA	0.02µA	600µA/160µA	PWM/PFM
LM2618 ATL	1.8V, 1.83V 1.87V, 1.92V	400mA/100mA	0.02µA	605µA/180µA	PWM/PFM
LM2619 ATL	1.5V – 3.6V	500mA/100mA	0.02µA	600µA/160µA	PWM/PFM

Synchronous Buck Converter



NMOS: synchronous rectifier

PMOS:
main switch

drivers

Switch
control
signals

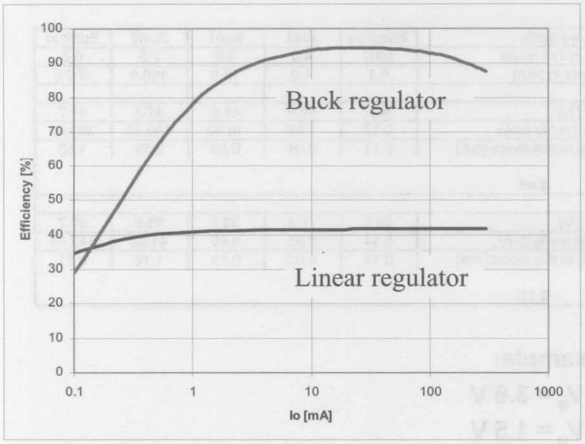
Dead times are
used to prevent
short-circuit current
through PMOS/NMOS

“dead” times

This slide shows the basic diagram of a buck converter implemented with PMOS and NMOS transistors. During the first part of the cycle the PMOS transistor is turned on and in the second part of the cycle the NMOS transistor is turned on. These MOSFETs are driven very hard, basically into their triode region, so when they’re turned on they look like very small resistances characterized by their RDSon. And it’s just RDSon combined with the current flowing through the switches that creates a loss which ends up giving somewhat less than 100 percent efficiency for the ideal converter. One thing you can notice here, if both the PMOS and NMOS were to be turned on at the same time, you’d have a very large amount of current flowing from the battery through ground. We want to avoid this, so essentially what we do is arrange the drive signals, as you can see at the lower part of the slides such that there’s a very small period of time called the “dead” time characterized here as td1 and td2 where both switches are turned off for a very short time during the transitions. During that time, the body diode of the NMOS transistor will have to turn on in order to take up the current from the inductor since the inductor will always try to maintain its current constant. The fact that the body diode is turning on is also another source of loss in a real practical converter. Switching losses also contribute to the losses.

On the output side we see a low-pass filter stage. The function of the output filter is to average out the rectangular waveform at the switching node (Vsw (t)) to a steady state DC voltage on the output. That’s what the load sees. The low-pass filter has a cutoff frequency that is much lower than the switching frequency and it allows the DC–DC voltage to appear on the output and filters away all the switching frequency and its harmonics.

SMPS Efficiency as a Function of Load



Example:

- $V_g = 3.6$ V
- $V_o = 1.5$ V
- $0 < I_o < 300$ mA

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Here we see a comparison for efficiencies between a linear regulator and a buck regulator over a comparable range of output currents.The output voltage here is 1.5V and we can see the linear regulator efficiency is only around 40% whereas buck converter efficiency is greater than 90% throughout most of the load ranges. If the output voltage requirement goes to 1.3V or 1.05V we can see that the linear regulator efficiency will be 30% or lower.

$$\eta_o = \frac{V_o I_o}{V_g I_g} = \frac{V_o I_o}{V_g (I_o + I_Q)} \qquad \eta_o < \frac{V_o}{V_g}$$

The formula above gives the efficiency for a linear regulator. Linear regulator efficiency cannot be greater than the ratio of the output and the input voltage.This is an important statement and we can see that is why we get a flat efficiency number over the entire output current range. The buck converter has a very high efficiency compared to linear regulators except for a small region at very light loads.This is because the quiescent current for buck converters is more than for linear regulators due to more active circuitry involved. However the evolution of modern buck converters with different modes of operation like pfm, burst, ldo modes etc are making the low-current efficiency of buck converters as good as that of linear regulators. Thus by using a buck converter with these modes in portable applications gives a much longer battery life by being efficient during low power standby modes and highly efficient during full power modes.

Impact of Efficiency: a System Example

	uP/DSP core mode	Stand-by	Wait	Run1	Run2	FullRun
	% of time in this mode	90.0	4.0	3.0	2.5	0.5
	Load current Io [mA]	0.1	1.0	10.0	100.0	300.0
Linear regulator	Efficiency [%]	34.7	40.9	41.6	41.7	41.7
	Battery current Ig [mA]	0.12	1.02	10.02	100.02	300.02
	Average Ig in this mode [mA]	0.11	0.04	0.30	2.50	1.50
Total linear reg average Ig [mA]	**4.45**					
SMPS	Efficiency [%]	29.1	78.4	93.7	93.0	87.7
	Battery current Ig [mA]	0.14	0.53	4.45	44.82	142.60
	Average Ig in this mode [mA]	0.13	0.02	0.13	1.12	0.71
Total SMPS average Ig [mA]	**2.12**					

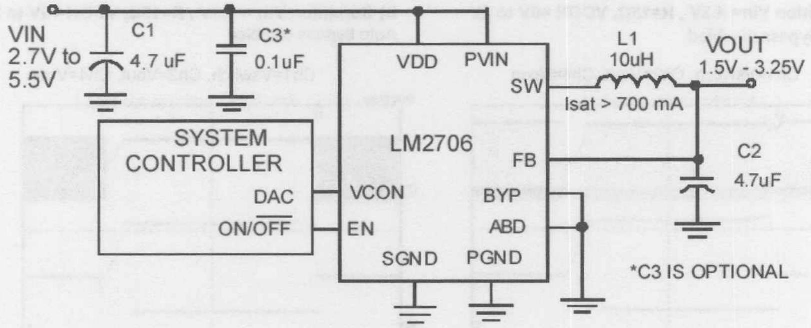
Example:

- $V_g = 3.6\ \text{V}$
- $V_o = 1.5\ \text{V}$
- $0 < I_o < 300\ \text{mA}$

Let's look at how these wonderful efficiency numbers for a buck converter can help us in real life. This is a slide showing the microprocessor DSP core operating either from a linear regulator or from a switch-mode power supply. What we see here is the microprocessor DSP core having different modes of operation such as Stand-by, Wait, Run1, Run2, and Full Run. And as we see here, the microprocessor DSP core spends 90 percent of its time in Stand-by mode and only around 0.5 percent of its time at the high output currents in the Full Run mode. We can calculate the average battery current drawn in each mode (by multiplying the battery current by the percentage of time it spends in that mode) and calculate the total average current drawn from the battery by summing up all the average currents for each mode. We see that the average current drawn from battery is 4.45 milliamps for the linear regulator whereas only 2.12 milliamps for the switch-mode power supply. This is a big advantage. One, it helps us to reduce the battery size for the same application, or two, it helps us to improve the battery life for the same application.

This advantage is in the case for a system spending 90% of its time in low-power standby mode where the buck converter is at a disadvantage compared to linear regulator (higher quiescent currents) so we can imagine the big advantage if the system spends a bigger percentage of time in the high-power modes.

RF PA Supply – LM2706

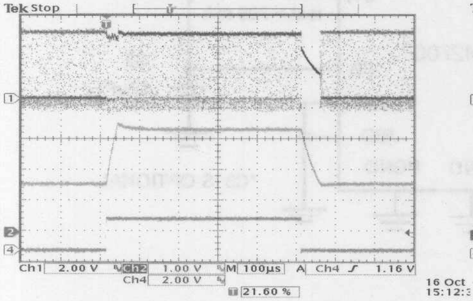


This is the typical application circuit for a RF PA buck converter. It can be seen that a DAC can control the output voltage of the converter between the levels of 1.5V and 3.25V.The LM2706 also has a bypass switch and auto bypass function to minimize the input to output dropout. The LM2706 can be used in any application that needs to change the output voltage of the converter dynamically by using a simple VCON signal.

WCDMA application

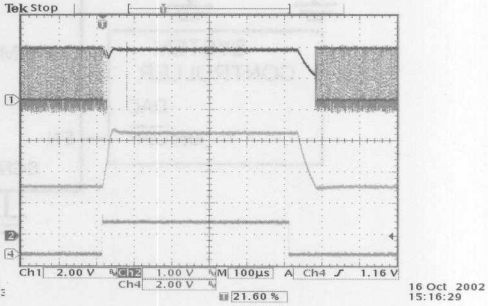
a) Condition Vin= 4.3V , R=15Ω, VCON =0V to 2V
Auto bypass disabled

Ch1=Vswitch, Ch2=Vout, Ch4=Vcon



b) Condition Vin = 3.3V , R=15Ω, VCON =0V to 2V
Auto bypass disabled

Ch1=Vswitch, Ch2=Vout, Ch4=Vcon



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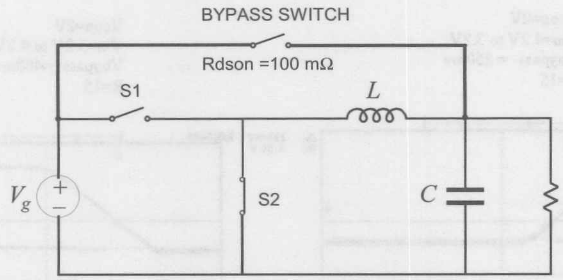
The plots show the typical application of the RF PA. The scope plot on the left shows the output voltage changed between 1.5V and 3.25V every 666 µs. It can be seen that the rise time for the output voltage is less than 30 µs.The plot on the right shows the same steps in output voltage for a lower battery voltage condition and it can be seen that when 3.25V is commanded the part goes into dropout and the PFET is on for 100% of the time.

Bypass Switch



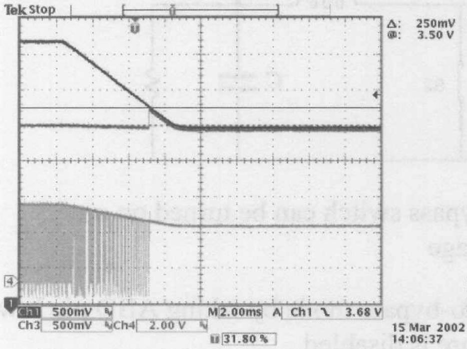
BYP : Using the BYP pin the bypass switch can be turned on or off irrespective of the input voltage

ABD: The part can be put in auto-bypass mode by taking ABD pin low; if it is high the auto bypass feature is disabled

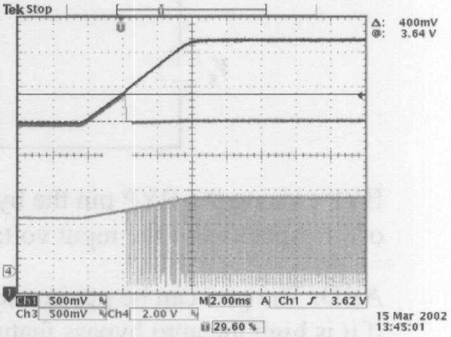
The advantage of using the bypass switch is evident from this figure. The bypass switch minimizes the drop across the input and output which in a conventional buck converter would be the Rdson of the PFET plus the dc resistance of the inductor. The bypass switch can be turned on or off using the bypass pin or it can be turned on automatically using the auto-bypass function.

Understanding Auto-bypass

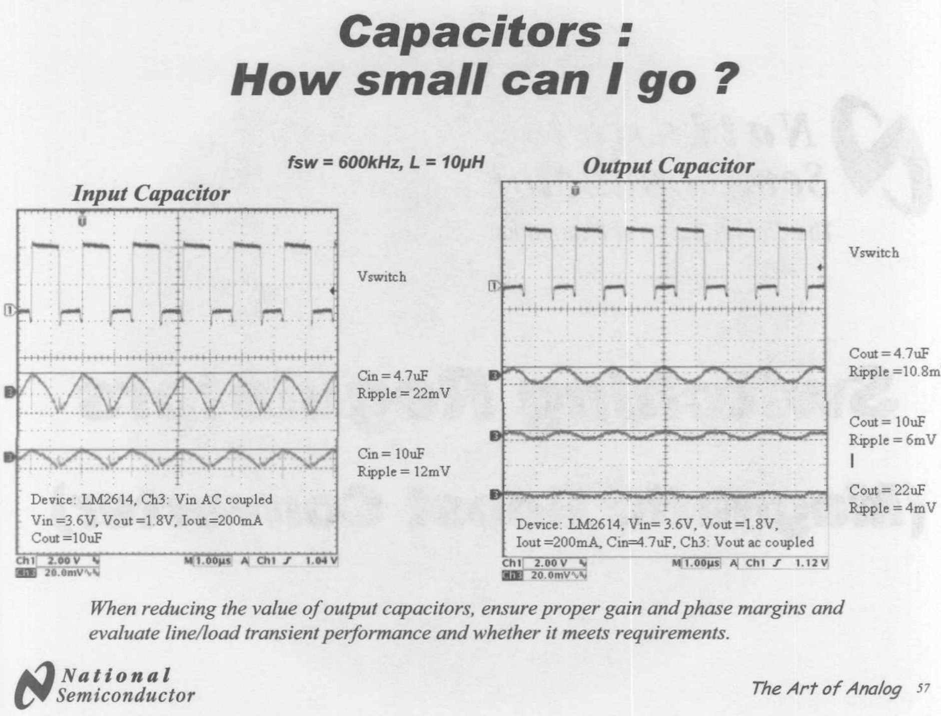
Vcon=2V
Vin=4.2V to 3.2V
Vbypass- = 250mv
R=15



Vcon=2V
Vin=3.2V to 4.2V
Vbypass+=400mv
R=15



The plots above show the detailed functioning of the auto bypass feature. When the auto-bypass function is enabled, it monitors the input voltage and when the input voltage crosses a threshold 250 mV above the set output voltage the bypass switch turns on and when the input voltage goes 400 mV above the set output voltage the bypass switch turns off.



Capacitors :
How small can I go ?

fsw = 600kHz, L = 10μH

When reducing the value of output capacitors, ensure proper gain and phase margins and evaluate line/load transient performance and whether it meets requirements.

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Buck converters have a higher input ripple current than output ripple current.This is evident from the plots above.When the same capacitance value is used for the input and output in identical conditions it is seen that the input voltage ripple is around two times the output voltage ripple.

Now let's look why the input ripple current is higher.

The ripple current flowing through the output capacitor is the inductor current ripple, but it's a different matter when we come to the input capacitor. When the PMOS is ON the current drawn from the battery is equal to the inductor current, so that's why we will see a slope. When the NMOS is on, the current drawn from the battery drops to zero. So we see that the input current is pulsating, and it has high ripple content. Naturally, the rms current for the input capacitor will be higher than the rms current for the output capacitor. That's why the use of input filter capacitors is mandatory in switching buck converters. It helps to reduce the input voltage noise and ensures proper operation of the device, and helps to prevent propagation of switching noise to other system components.

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Switching Regulators

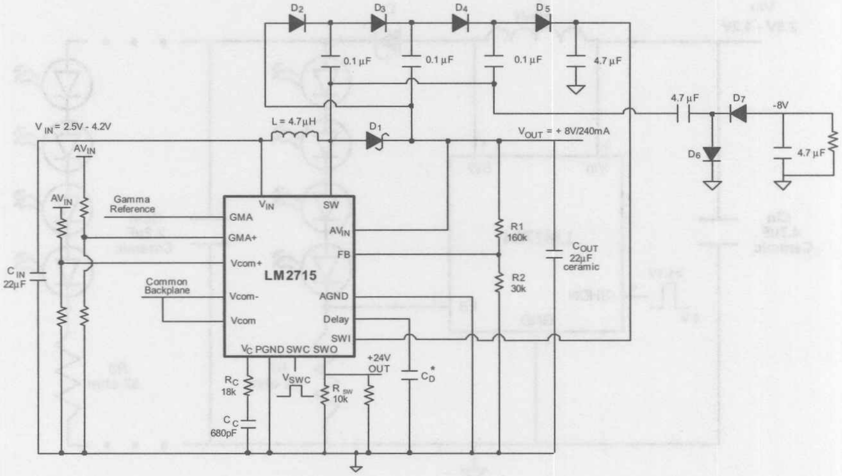
(Magnetic Boost Converter)

Boost Converters Selection Guide

Parameter	LM2703	LM2704	LM2705	LM3500	LM3501
Operation	PFM	PFM	PFM	PWM	PWM
Switching Frequency (OFF Time)	(400ns)	(400ns)	(400ns)	1MHz	1MHz
Synchronous?	NO	NO	NO	YES	YES
True Shutdown? (Vout = 0V)	NO	NO	NO	YES	YES
PWM Brighness Control? (via SD)	YES	YES	YES	YES	YES
Analog Voltage Brightness Control?*	NO	NO	NO	NO	YES
Input UVLO?	YES	YES	YES	YES	YES
Output OVP?	NO	NO	NO	YES	YES
Input Voltage Range	2.2V to 7V	2.2V to 7V	2.2V to 7V	2.7V to 7V	2.7V to 7V
Max. Switch Voltage	20.5V	20.5V	20.5V	15.5V	15.5V
Switch Current Limit	350mA	550mA	150mA	400mA	400mA
Power Switch Rdson	0.7ohm	0.7ohm	0.7ohm	0.4ohm	0.4ohm
Feedback Voltage	1.26V	1.26V	1.26V	0.5V	0.05V to 0.5V*
3 LED Efficiency, 20mA, 3.3V in**	77%	77%	76% (at 10mA)	81%	80%
No Load Switching Iq	235uA	235uA	235uA	1.5mA	2mA
Package	SOT23-5	SOT23-5	SOT23-5	Thin micro SMD 8	Thin micro SMD 8

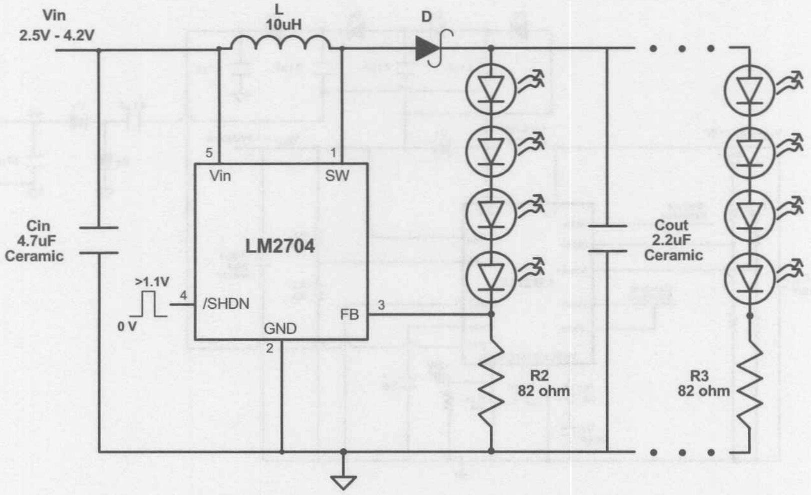
*Analog brightness achieved by varying the FB voltage via an analog signal on the CNTRL pin.
**Efficiency into LEDs, current set resistor is viewed as a loss.

LM2702/10/11



- PWM (Pulse Width Modulated) Boost converters for TFT LCD drive.
- Input range 2.2V to 12V (2.2V to 7.5V for the ’10 and ’11)
- Ideal for driving large TFT LCDs that require multiple voltages
- High current limit of 2A (1.4A for the ’10 and ’11).
- LM2702 adds a Vcom amplifier for the common backplane, a Gamma buffer for the column drivers and an internal controllable PMOS switch for row control.
- LM2711 adds 4 Gamma buffers for the column drivers and the LM2710 adds an additional Vcom buffer.
- TSSOP packages and high frequency operation (600 kHz for the ’02, 600 kHz or 1.25 MHz selectable for the ’10 and ’11) for small, thin solution size

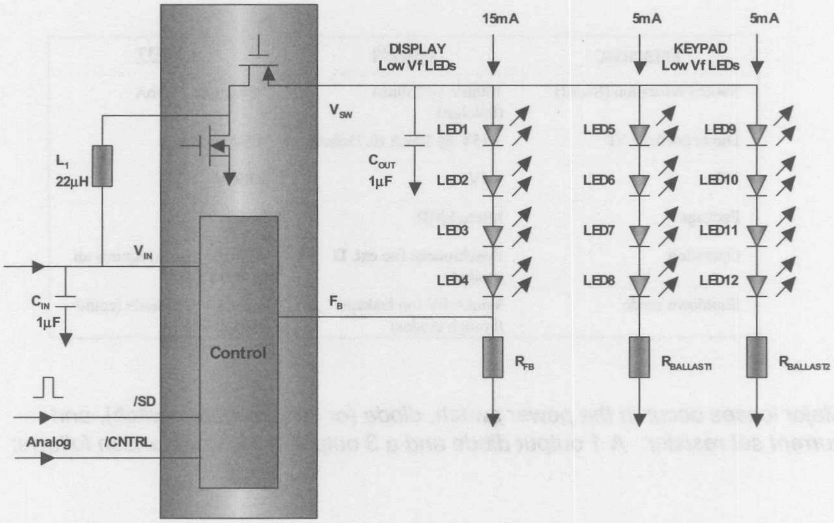
LM2704 Magnetic Driver



- •PFM (Pulse Frequency Modulated) Boost converters for high efficiency conversion
- Input range 2.2V to 7V, output up to 20V
- Ideal for driving white LEDs, up to 4 in series at 20 mA (8, 2 strings of 4 in series at 20 mA each for the LM2704)
- Current limit 150 mA ('05), 350 mA ('03), 550 mA ('04)
- Low current limit makes LM2705 ideal for current limited USB applications
- SOT-23 package and small surface mount inductor and ceramic capacitors for overall compact solution size.
- BRGT pin offers analog brightness control, SD offers digital control (PWM)
- Efficiency of constant current is same as efficiency of volt. mode total solution if you take ballast R's into account.

# of LEDs	LM2703	LM2704
2	30mA each	60mA each
3	20mA each	40mA each
4	15mA each	30mA each
6	10mA each	20mA each
8	8mA each	15mA each

Magnetic Boost LED Driver



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- PWM (Pulse Width Modulated) synchronous boost converters for white LED drive.
- Input range 2.2V to 6V, output up to 15V
- Ideal for driving white LEDs, up to 4 (low Vf) in series or 8, 2 strings of 4 in series.
- 500 mA switch current limit and true shutdown capability (Vout = 0V).
- Synchronous operation and low feedback voltage for high efficiency conversion
- SOT-23 package and small surface mount inductor and ceramic capacitors for overall compact solution size.
- LM3501 adds analog LED current control via a CNTRL pin, an applied analog voltage varies the feedback voltage.

The Efficiency, A Comparison

Parameter	LM3500	LT1937
Switch saturation (Swsat)	100mV @ 250mA (0.4ohm)	350mV @ 250mA
Diode (switch) Vf	.015V @ 20mA (0.75ohm)	0.5V @ 20mA
Vfb	0.5V	0.095V
Package	Micro SMD	SC70
Operation	Synchronous (no ext. D needed)	Asynchronous (requires an external D)
Shutdown mode	Vout = 0V (no leakage through diodes)	Vout = Vin-Vdiode (could have leakage)

Major losses occur in the power switch, diode (or synchronous switch), and current set resistor. A 1 output diode and a 3 output diode comparison follows:

Losses (Approximate) 1 LED @ 20 mA, Vin= 3.3V

LM3500	LT1937
Vout = 4.1V	Vout = 3.7V
D = 0.195	D = 0.108
Iin = 25mA (approx)	Iin = 25mA (approx)
Swsat = 10mV (Iin*Rdson)	Swsat = 200mV (assumed minimum, bipolar)
Pswitch = 0.05mW	Pswitch = 0.54mW
Pdiode = 0.3mW	Pdiode = 10mW
Presistor = 10mW	Presistor = 1.9mW
Ploss = 10.35mW	**Ploss = 12.44mW**

Pswitch = D x Swsat x Iin, Pdiode = Vf x Iout, Presistor = Vfb x Iout

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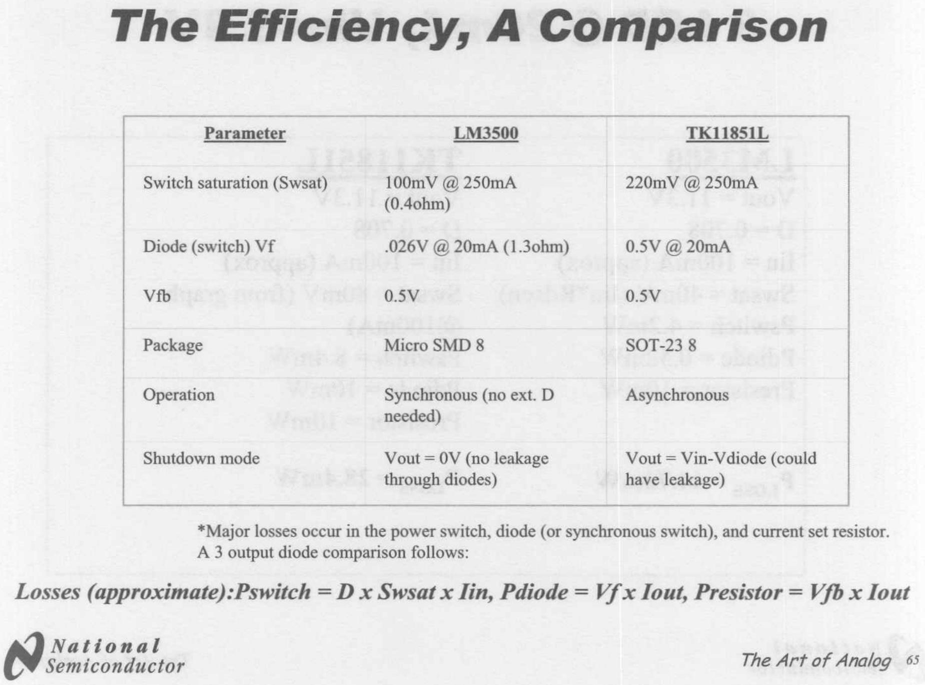
Losses (Approximate) 3 LED @ 20 mA, Vin= 3.3V

LM3500	**LT1937**
Vout = 11.3V	Vout = 10.9V
D = 0.708	D = 0.697
Iin = 100mA (approx)	Iin = 100mA (approx)
Swsat = 40mV (Iin*Rdson)	Swsat = 250mV (assumed minimum, bipolar)
Pswitch = 2.8mW	Pswitch = 17.4mW
Pdiode = 0.3mW	Pdiode = 10mW
Presistor = 10mW	Presistor = 1.9mW
P_{LOSS} = 13.1mW	**P_{LOSS} = 29.3mW**

Pswitch = D x Swsat x Iin, Pdiode = Vf x Iout, Presistor = Vfb x Iout

These are approximate equations but easily show how the low Rdson and synchronous architecture of the LM3500 more than make up for the efficiency loss due to a higher feedback voltage.

LM3500 also offers true shutdown and no external diode requirement.



The Efficiency, A Comparison

Parameter	LM3500	TK11851L
Switch saturation (Swsat)	100mV @ 250mA (0.4ohm)	220mV @ 250mA
Diode (switch) Vf	.026V @ 20mA (1.3ohm)	0.5V @ 20mA
Vfb	0.5V	0.5V
Package	Micro SMD 8	SOT-23 8
Operation	Synchronous (no ext. D needed)	Asynchronous
Shutdown mode	Vout = 0V (no leakage through diodes)	Vout = Vin-Vdiode (could have leakage)

*Major losses occur in the power switch, diode (or synchronous switch), and current set resistor. A 3 output diode comparison follows:

Losses (approximate):Pswitch = D x Swsat x Iin, Pdiode = Vf x Iout, Presistor = Vfb x Iout

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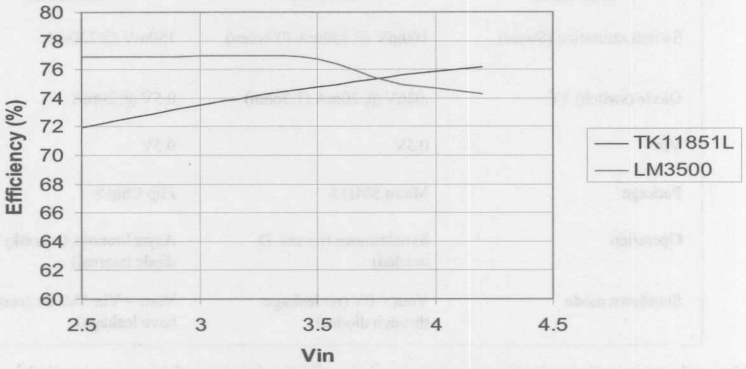
Please note the significant differences in switch saturation voltage and the voltage across the diode.

3 LED @ 20mA, Vin=3.3V

LM3500	**TK11851L**
Vout = 11.3V	Vout = 11.3V
D = 0.708	D = 0.708
Iin = 100mA (approx)	Iin = 100mA (approx)
Swsat = 40mV (Iin*Rdson)	Swsat = 80mV (from graph @100mA)
Pswitch = 4.2mW	Pswitch = 8.4mW
Pdiode = 0.52mW	Pdiode = 10mW
Presistor = 10mW	Presistor = 10mW
P_{LOSS} = 14.72mW	**P_{LOSS} = 28.4mW**

Efficiency Comparison



Note 1: *The LM3500 uses the DT1608C-222 inductor with 200 mΩ ESR. The TK11851L uses a D52LC inductor (Toko) with 250 mΩ ESR. Both were measured on the bench.*

Note 2: *Notice the graph on the front page of the TK11851L datasheet. It represents the standard Pout and does not count the Rset*Iled as a loss.*

The Efficiency, A Comparison

Parameter	**LM3500**	**TK11860B**
Switch saturation (Swsat)	100mV @ 250mA (0.4ohm)	150mV @ 250mA
Diode (switch) Vf	.026V @ 20mA (1.3ohm)	0.5V @ 20mA
Vfb	0.5V	0.5V
Package	Micro SMD 8	Flip Chip 8
Operation	Synchronous (no ext. D needed)	Asynchronous (schottky diode internal)
Shutdown mode	Vout = 0V (no leakage through diodes)	Vout = Vin-Vdiode (could have leakage)

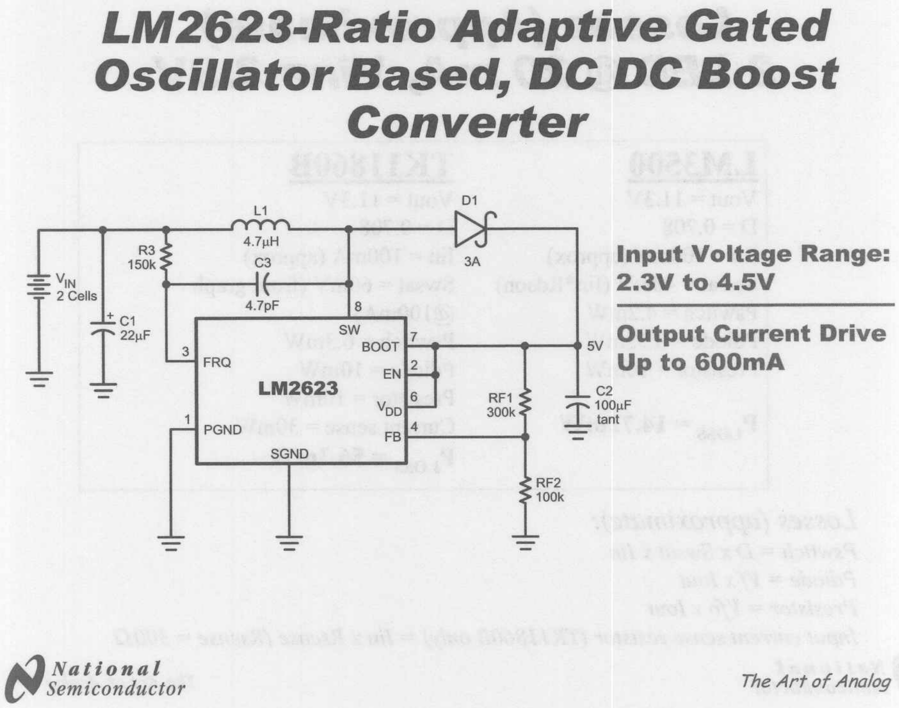
Major losses occur in the power switch, diode (or synchronous switch), and current set resistor with the TK11860B adding another major loss in the form of a current sense resistor connected between Vin and Is (where the inductor connects).

Losses (Approximate)
3 LED @ 20 mA, Vin= 3.3V

LM3500	**TK11860B**
Vout = 11.3V	Vout = 11.3V
D = 0.708	D = 0.708
Iin = 100mA (approx)	Iin = 100mA (approx)
Swsat = 40mV (Iin*Rdson)	Swsat = 60mV (from graph @100mA)
Pswitch = 4.2mW	Pswitch = 6.3mW
Pdiode = 0.52mW	Pdiode = 10mW
Presistor = 10mW	Presistor = 10mW
	Current sense = 30mW
P_{LOSS} = 14.72mW	**P_{LOSS} = 56.3mW**

- *Losses (approximate):*

Pswitch = D x Swsat x Iin
Pdiode = Vf x Iout
Presistor = Vfb x Iout
Input current sense resistor (TK11860B only) = Iin x Rsense (Rsense = 300Ω



LM2623-Ratio Adaptive Gated Oscillator Based, DC DC Boost Converter

Input Voltage Range: 2.3V to 4.5V

Output Current Drive Up to 600mA

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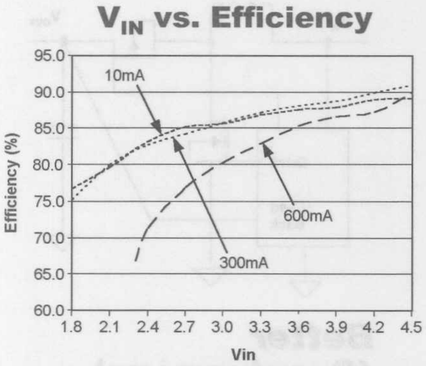
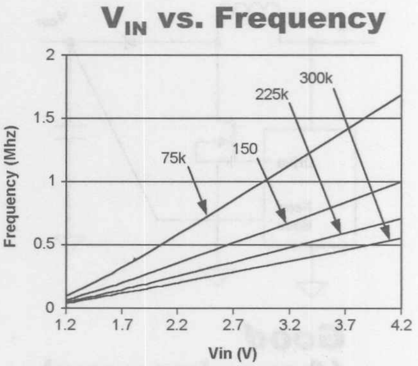
The LM2623 is a high-efficiency, general-purpose, step-up DC-DC switching regulator for battery-powered and low input voltage systems. It accepts an input voltage between 0.8 and 14 volts and converts it into a regulated output voltage between 1.24 and 14 volts. Efficiencies up to 90% are achievable with the LM2623.

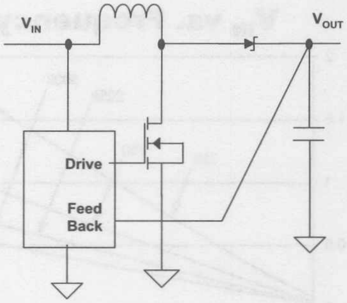
- Good efficiency over a very wide load range
- Very low output voltage ripple
- Small, mini-SO-8 package (half the footprint of standard 8 pin SO package)
- 1.09 mm package height
- Up to 2 MHz switching frequency
- 0.8V to 14V operating voltage
- 1.1V start-up voltage
- 1.24V - 14V adjustable output voltage
- Up to 2A load current at low output voltages
- 0.17W internal MOSFET
- Up to 90% regulator efficiency
- 80 µA typical operating current (into VDD pin of supply)
- <2.5 µA guaranteed supply current in shutdown
- 4 mm x 4 mm LLP package option

Performance Curves

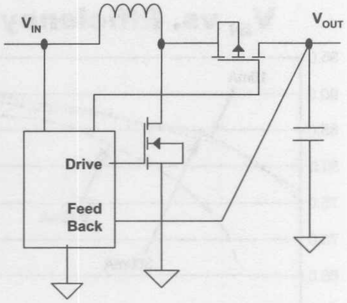

V_{IN} vs. Efficiency


V_{IN} vs. Frequency

“Boosting“ the Efficiency



Good (Asynchronous)



Better (Synchronous)

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Asynchronous operation requires an external Schottky diode, however the control circuitry is more simple. More simple control circuitry and the lack of a second on-chip power switch results in smaller die area and lower IC cost.

Synchronous operation integrates a power switch to take the place of the Schottky diode. This results in higher efficiency, the possibility of true shutdown (Vout=0V in shutdown), and smaller solution size at the cost of a larger die and higher IC cost.

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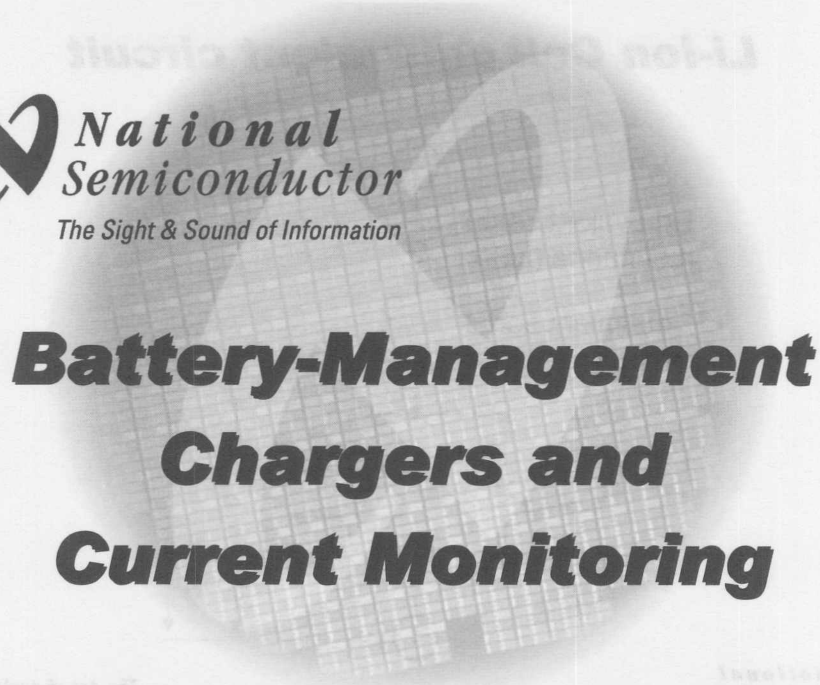
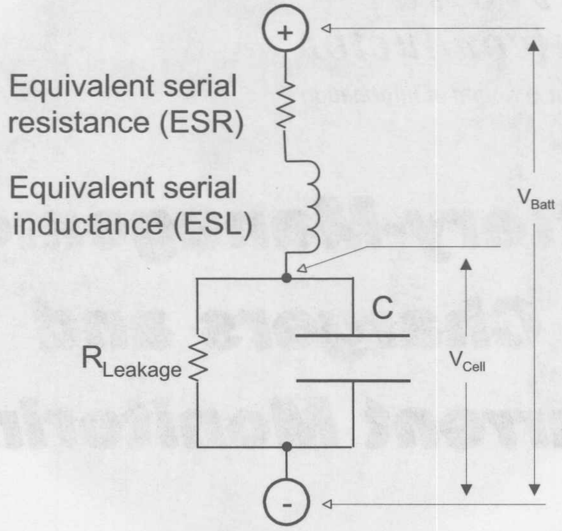


Battery-Management Chargers and Current Monitoring

Li-Ion Cell equivalent circuit


+
Equivalent serial resistance (ESR)
Equivalent serial inductance (ESL)
C
R_Leakage
V_Batt
V_Cell
-

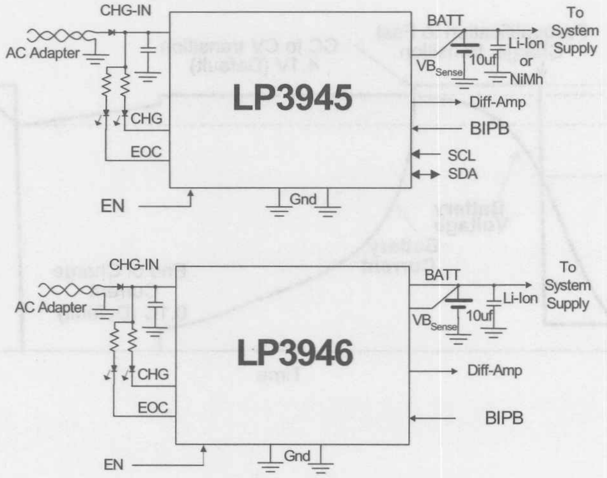
A battery's simulation model is shown here. ESR and ESL are a function of the battery's mechanical construction. ESL is in the nH range and ESR is anywhere between 50 to 150 milliohms.

Depending on age, temperature and condition of the battery, ESR varies significantly.

$R_{Leakage}$ is the internal leakage of the battery. The charge storage characteristic of the battery is modeled by a LLLAAARRRGE capacitor.

The ESR is most troublesome in terms of charging since it creates an error between the actual cell voltage and the battery terminal voltage. Accurate control of the voltage across the cell is the most important parameter in accurately and safely charging a Li-Ion battery.

LP3945/46
Battery-Charge Management System



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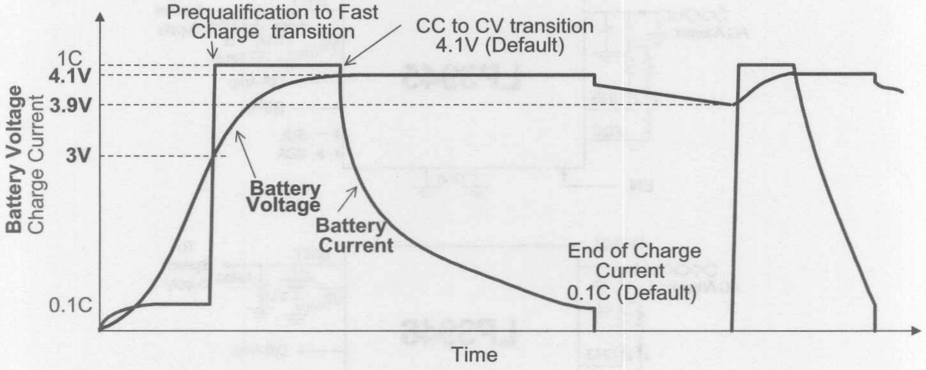
The Art of Analog 75

- Integrated pass transistor
- Does not require external charge current setting resistor
- I^{2}C interface (LP3945 only) - programmable charge current, EOC current and battery regulation voltage and battery type.
- For lp3946, charge current, termination voltage and EOC default values are set at the factory per customer specifications.
- Near-depleted battery preconditioning
- Built-in 5.6 hour timer
- Under voltage and over voltage lockout
- Charge status indicators
- Charge current monitor output
- LDO mode operation can source 1 Amp
- Continuous over-current / temperature protection

LP3945/46 Charge Cycle



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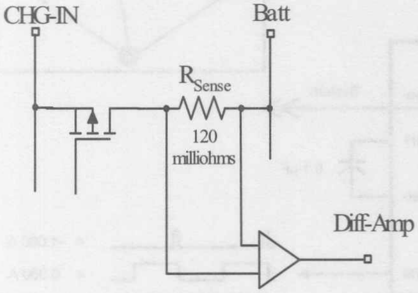
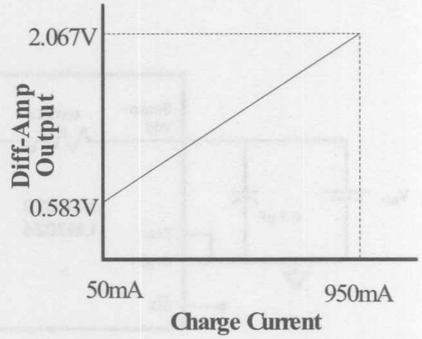
The Art of Analog 76

The LP3945/46 charging profile shown here in this graph, contains battery conditioning and qualification phase, Constant Current (CC), Constant Voltage (CV) and maintenance phase. During the maintenance phase, battery voltage is monitored and charge cycle re-starts if it drops below 3.9 V

Charging is considered complete when charge current dropped to below 0.1 C during the CV phase.

LP3945/46
Charge Current Monitoring Circuit





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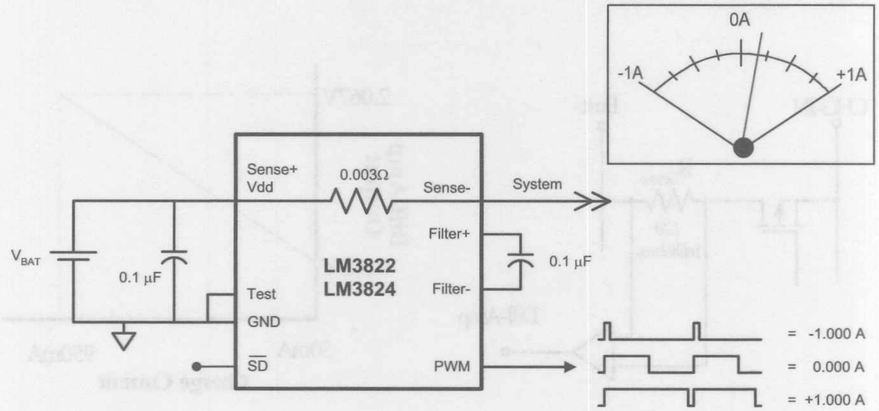
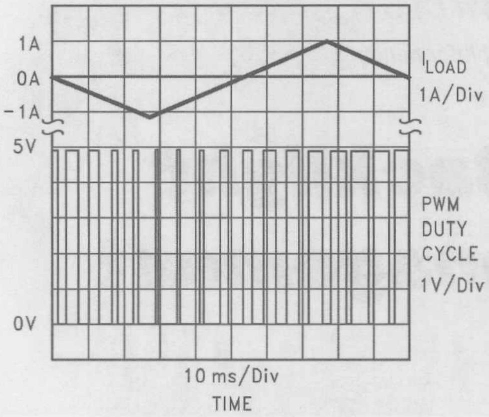
The charge current can be monitored continuously using the Diff-Amp output pin which is an analog presentation of the charge current. Its transfer function is shown here. The major advantage of this approach is the fact that by monitoring the charge current during the CV phase, a fairly accurate estimate of time-to-full-charge can be extracted.

LM3822/3824: Precision Current Gauges

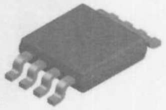


LM3822/3824: Precision Current Gauges

Input/Output Characteristics



Mini-SO (MSOP) package



3mm × 5mm × 1.1mm

Recommended application: battery fuel gauge

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Part Option	Current Range	T_{MEAS}	Accuracy
LM3822-1.0	-1.0A to +1.0A	50 msec	± 2% / ± 4%
LM3822-2.0	-2.0A to +2.0A	50 msec	± 2% / ± 4%
LM3824-1.0	-1.0A to +1.0A	6 msec	± 3% / ± 5%
LM3824-2.0	-2.0A to +2.0A	6 msec	± 3% / ± 5%

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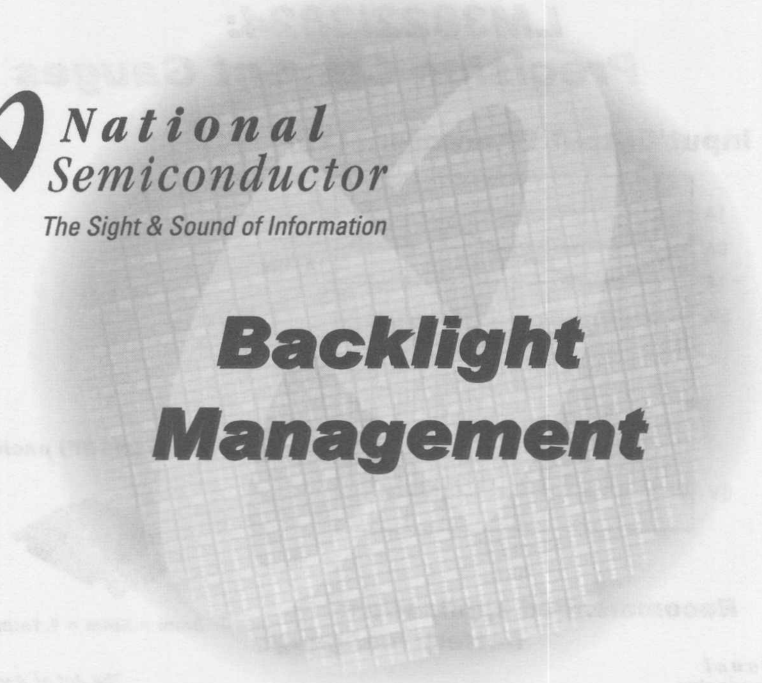
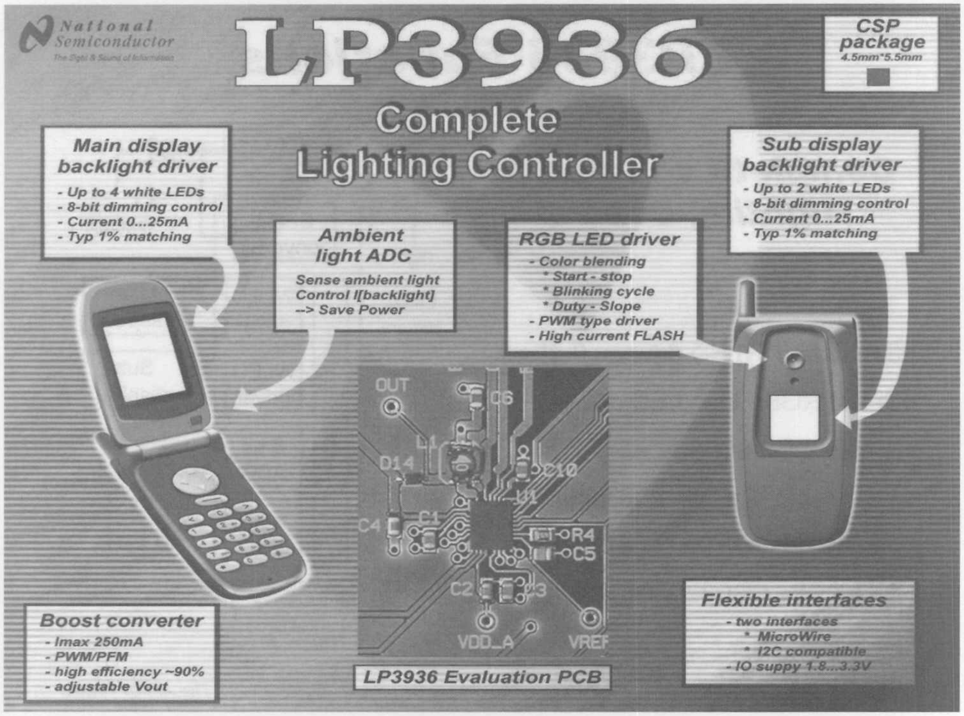


Backlight Management



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LP3936

Complete Lighting Controller

CSP package
4.5mm*5.5mm

Main display backlight driver
- Up to 4 white LEDs
- 8-bit dimming control
- Current 0...25mA
- Typ 1% matching

Ambient light ADC
Sense ambient light
Control I[backlight]
--> Save Power

RGB LED driver
- Color blending
  * Start - stop
  * Blinking cycle
  * Duty - Slope
- PWM type driver
- High current FLASH

Sub display backlight driver
- Up to 2 white LEDs
- 8-bit dimming control
- Current 0...25mA
- Typ 1% matching

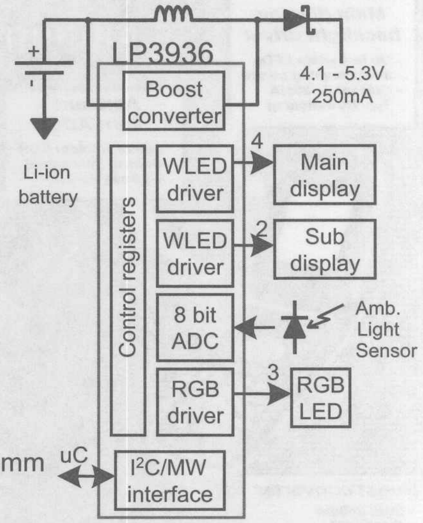
Boost converter
- Imax 250mA
- PWM/PFM
- high efficiency ~90%
- adjustable Vout

LP3936 Evaluation PCB

Flexible interfaces
- two interfaces
  * MicroWire
  * I2C compatible
- IO suppy 1.8...3.3V

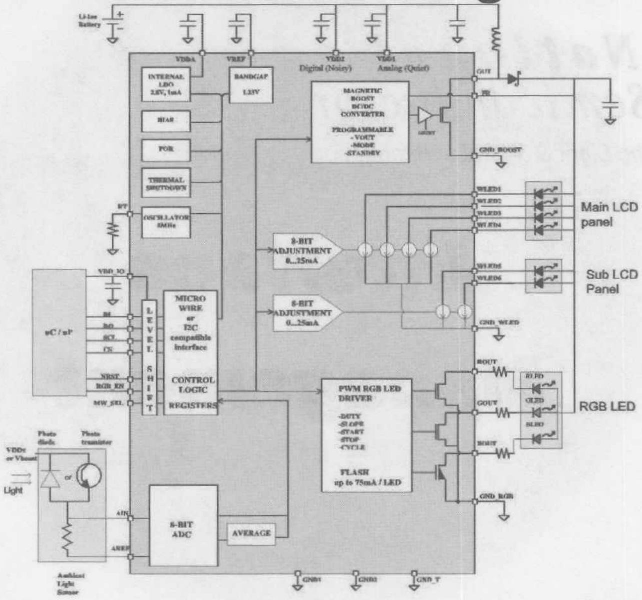
LP3936 Functions

Complete solution for lighting control



- 6 matched WLED drivers, 0-25mA
- Smart RGB/Flash LED driver
- Ambient light sensor ADC
- Adjustable high eff. boost converter
- I^{2}C and MicroWire serial interface
- Small size CSP32 package, 4.5 x 5.5mm

LP3936 Block Diagram



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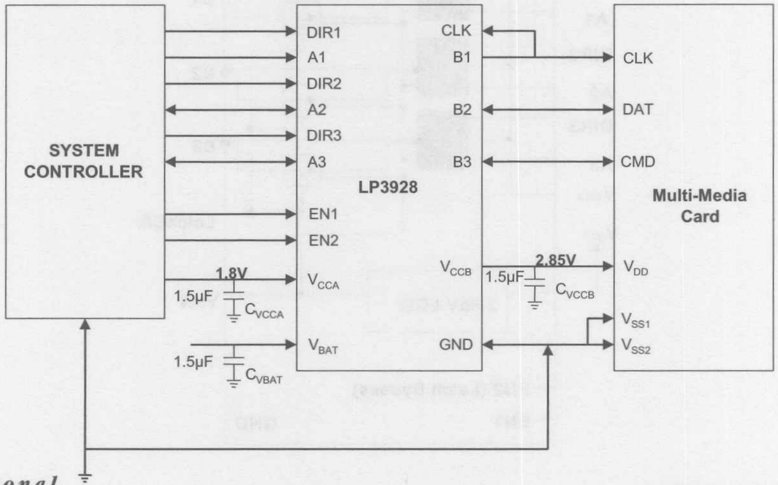
Interface Management

LP3928 High-Speed Bi-Directional Level Shifter + Ultra Low-Dropout CMOS Voltage Regulator



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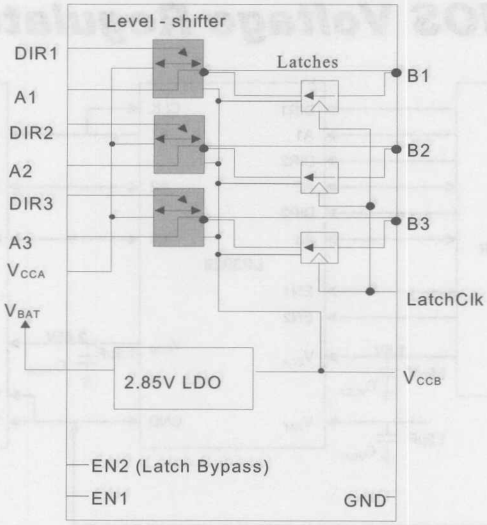
The Art of Analog 85

- High-performance three-signal level-shifter with 4 ns (typical) propagation delay
- 20 ns direction switch delay
- Individual direction control for the three level-shifted signals
- The three level-shifted signals can be latched or put into pass-through mode
- 2.8V, 150 mA CMOS linear regulator for supplying shifting level
- Linear regulator dropout voltage = 60 mV (typical) at full load of 150 mA
- 16 bump thin micro SMD package

LP3928 Functional Block Diagram



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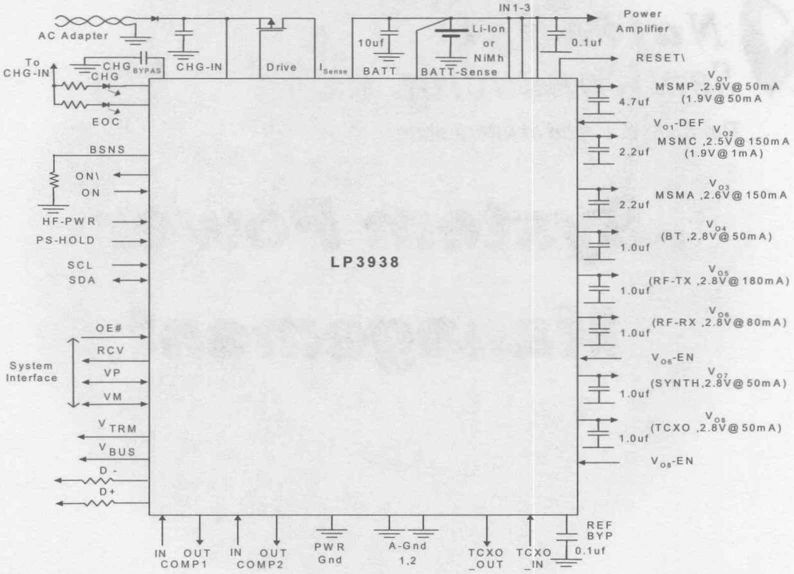
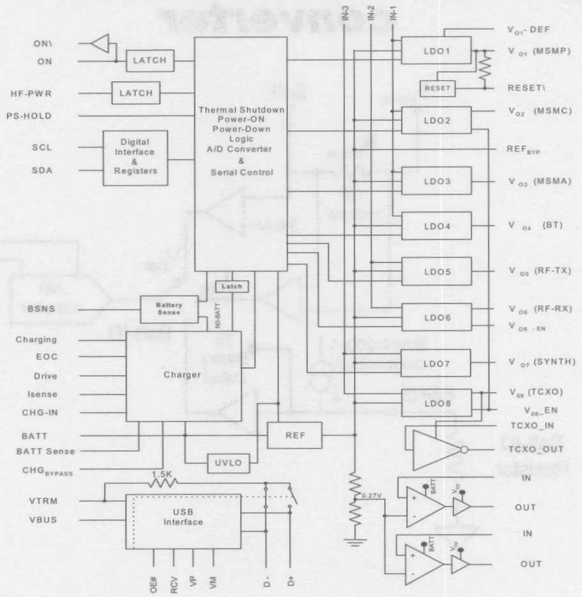
System Power Management

LP3938 Typical Application Circuit



- Eight low dropout, low noise LDO’s, two with idle mode
- Integrated TCXO buffer
- A constant-current/constant-voltage battery charger controller with charge status indicators.
- A Universal Serial Bus (USB) transceiver supporting Low-Speed and Full-Speed (12Mb/s) operation
- Smart battery detection circuit.
- I^2C serial interface for maximum flexibility

LP3938 Functional Block Diagram



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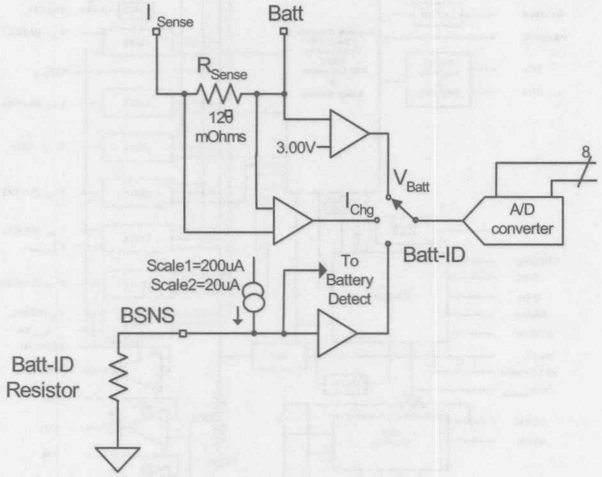
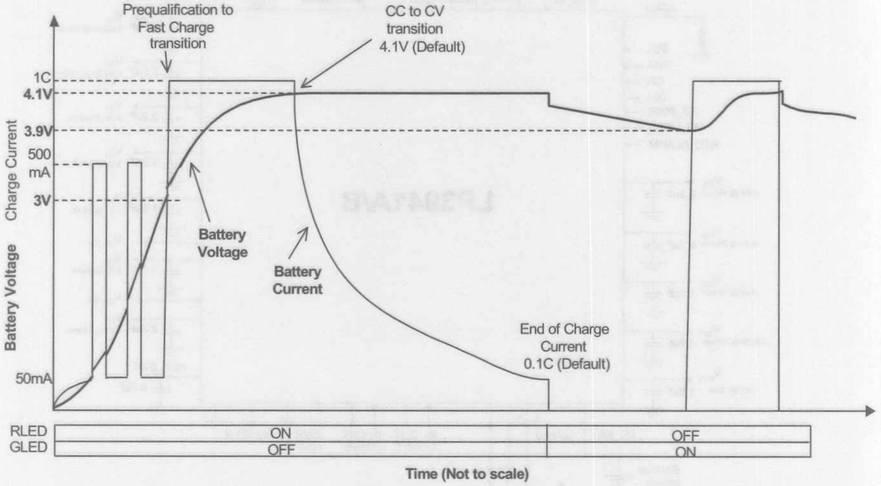
Battery ID Detection and A/D converter



LP3938 Charge and Maintenance Cycle



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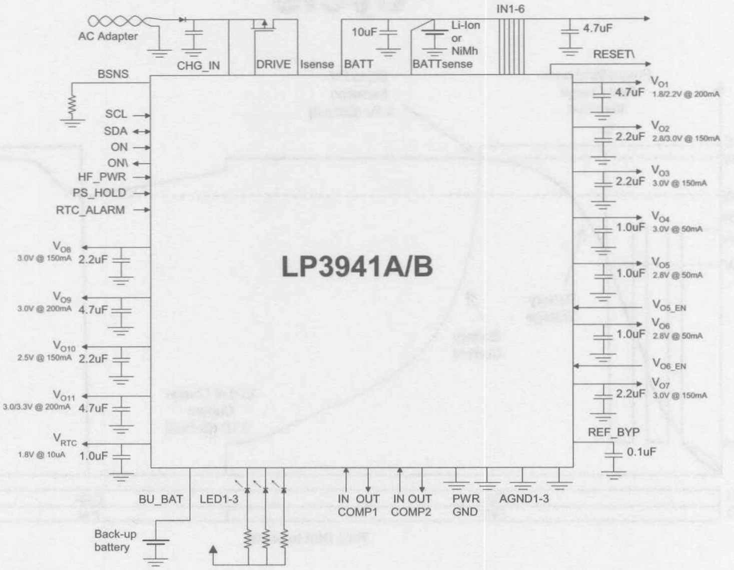
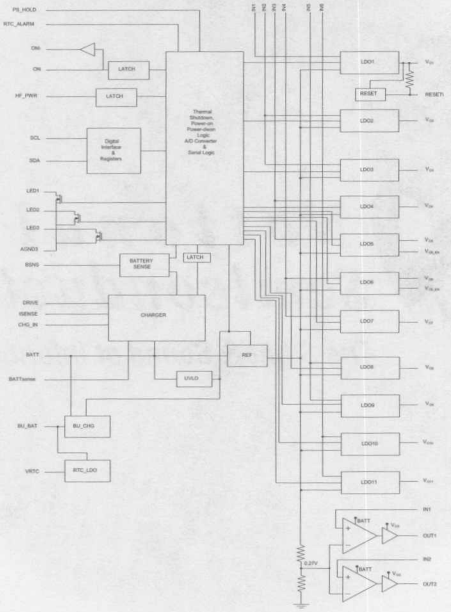
LP3941 Typical Application Circuit



- 11 low dropout, low noise LDOs.
- Dedicated low current LDO for real time clock supply.
- Back-up battery charger.
- A constant current / constant voltage battery charger controller with charge status indication via I^2C.
- Three open drain drivers to control a RGB LED.
- I^2C serial interface for maximum flexibility.

LP3941 Circuit Block Diagram



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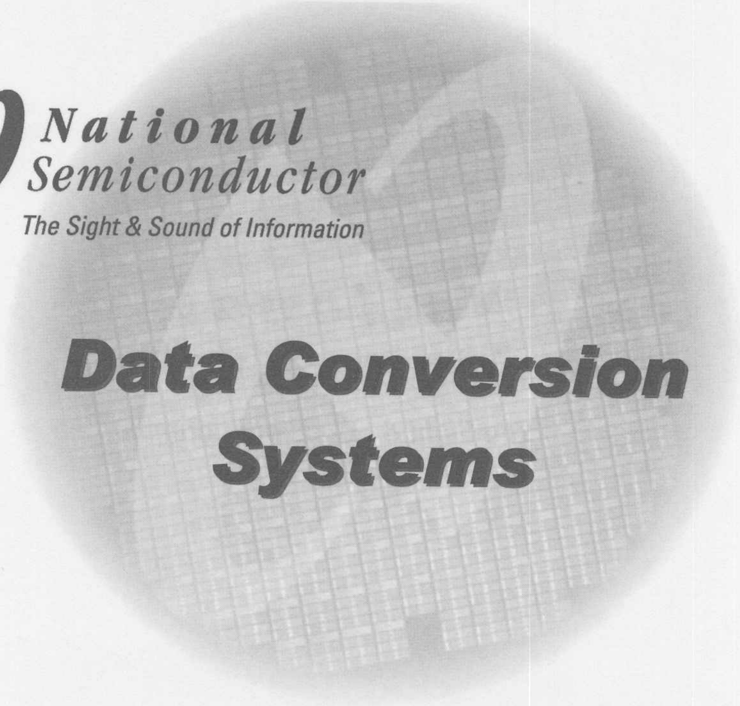

Data Conversion Systems

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The Sight & Sound of Information

Data Conversion Systems

- Thermal management
  - *Thermostats*
  - *Remote diode temperature sensors*
  - *Hardware monitors*
  - *SensorPath™ bus overview*
- Adcs
  - *Nomenclature*
  - *Output timing*
  - *High-speed clock considerations*
  - *Undersampling & aliasing*
  - *Developing a common mode voltage*

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The Art of Analog 3

Today's Data Conversion Systems agenda is rather broad, so you can understand that we will not exhaust the subject. We will, however, provide you with useful information.

National Semiconductor is a recognized leader in Thermal Management technology and offers such a wide range of solutions in that arena that we cannot cover all of them in this short time. The SensorPath™ Bus introduced here is an innovative single-wire bus developed for temperature sensors.

While National Semiconductor may not be the first name that comes to your mind when you think of ADCs (Analog-to-Digital Converters), we are widening our range of ADCs and believe that it is in your best interest to look at our offerings when you have a need in this area.

While we have not had many DACs (Digital-to-Analog Converters) for some time, we have plans to improve this area of our offerings: watch us grow!

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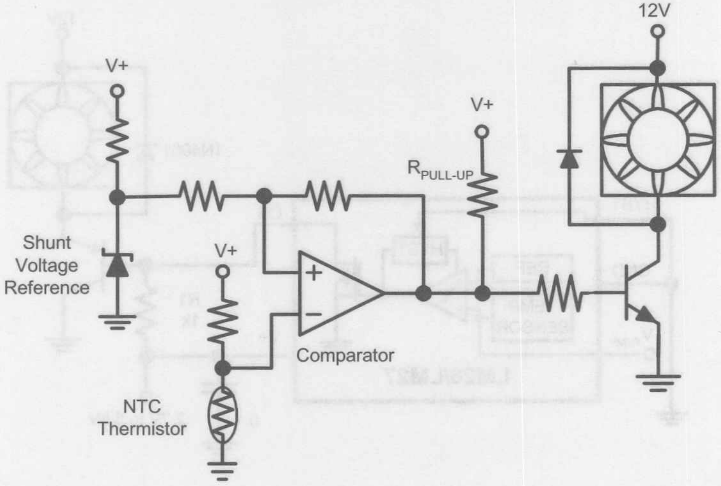
The Sight & Sound of Information

Themal Management:

Electronic Thermostats

Building an electronic thermostat from discrete components is not generally considered the best approach because of the direct cost involved. National Semiconductor has solutions that ease the design task while lowering design time and the real product cost.

Thermistor-Based Thermostat Circuit for Fan Activation



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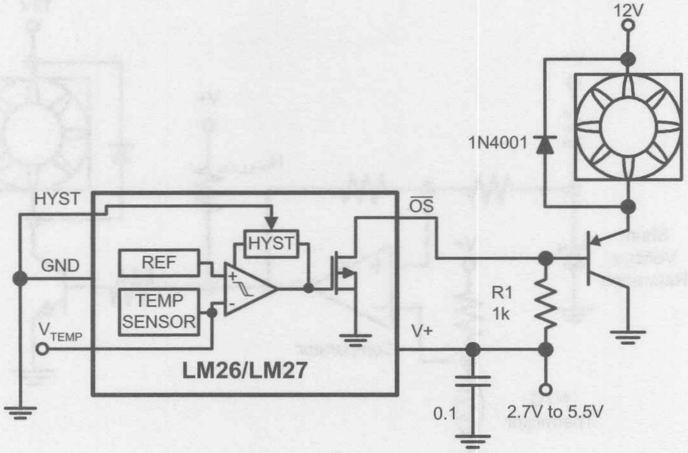
The Art of Analog 5

As an example of a discrete, non-integrated thermostat implementation, this conceptual circuit shows a topology that would activate a fan when a system's temperature exceeds a certain value. An appropriate thermistor is selected based on the performance desired (e.g. accuracy, linearity, etc.). As the temperature increases, the resistance of the negative-temperature-coefficient (NTC) thermistor decreases, causing the voltage at the thermistor and the inverting input to the comparator to decrease with it. The voltage (V_{TRIP}) would be calculated to correlate to the desired temperature (T_{TRIP}) at which the fan is to turn on. A small amount of positive feedback is added to provide some input hysteresis.

A voltage reference is selected to provide a voltage, equal to V_{TRIP}, to the non-inverting input of the comparator. At measured system temperatures below T_{TRIP}, the voltage at the inverting input would be greater than reference voltage so the output signal from the comparator would be low. Once the system temperature exceeds T_{TRIP}, the voltage at the inverting input would be greater than the reference voltage, causing the comparator output to go high, thus turning on the transistor switch and the fan.

Some limitations of this topology include the accuracy of the thermistor, the accuracy of the other discrete components over temperature, and the relatively high number of components.

LM26/LM27 Thermostat for Fan Activation



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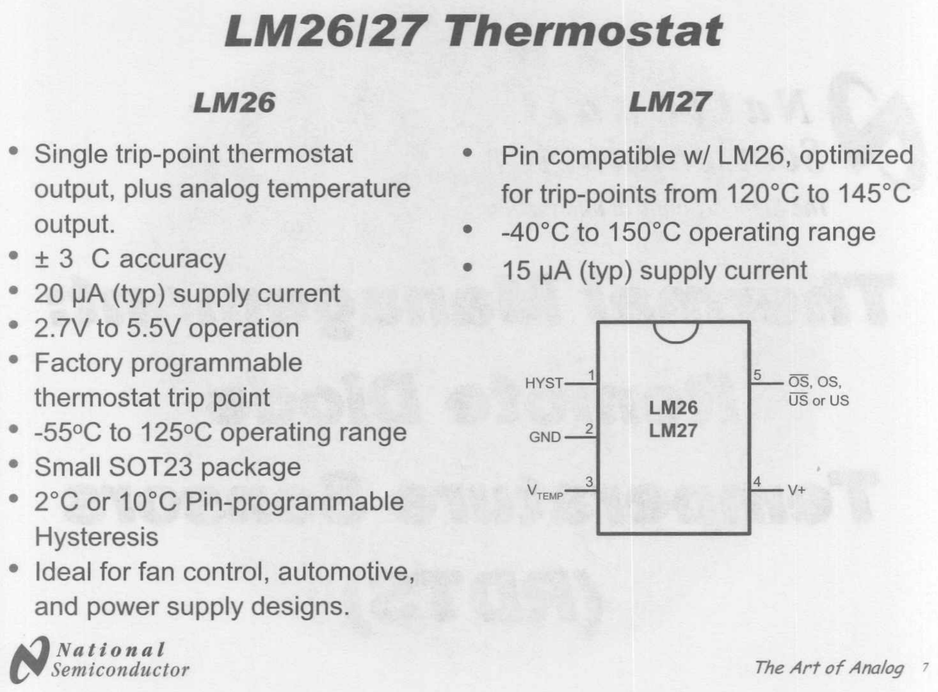
The LM26 and LM27 are integrated circuit thermostats that provide all of the functionality of the previous discrete circuit, plus many feature and performance improvements – including excellent accuracy, low supply current, and wide operating voltage range – in a small SOT23 package. Both the LM26 and the LM27 eliminate the component count, board area, and design effort associated with a discrete circuit.

This application shows an LM26/LM27 with an active-low output which triggers on an over-temperature event, turning on the switch and thus the fan (in this circuit, the fan is a Toyo USTF802512HW). Another application would be to connect the output of an LM26/LM27 to a microprocessor input for system monitoring of an over-temperature or under-temperature alarm. The LM26/LM27 temperature trip point (TTRIP) can be preset at the factory, in 1°C increments, to any temperature within a wide range: -55°C to +110°C for the LM26 and +120°C to +150°C for the LM27. These thermostats are available in active-high or active-low outputs. The hysteresis is pin-selectable for 2°C or 10°C. The LM26 and LM27 are also available to trigger on either a positive-going temperature (to signal an over-temperature event) or a negative-going temperature (for an under-temperature event). The output VTEMP provides an analog voltage which is proportional to temperature. This output can be used elsewhere in the system (an input to an ADC, for example) and/or can be used as test pin during system testing.



LM26/27 Thermostat

LM26

- Single trip-point thermostat output, plus analog temperature output.
- ± 3 C accuracy
- 20 µA (typ) supply current
- 2.7V to 5.5V operation
- Factory programmable thermostat trip point
- -55^{o}C to 125^{o}C operating range
- Small SOT23 package
- 2°C or 10°C Pin-programmable Hysteresis
- Ideal for fan control, automotive, and power supply designs.

LM27

- Pin compatible w/ LM26, optimized for trip-points from 120°C to 145°C
- -40°C to 150°C operating range
- 15 µA (typ) supply current

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The Art of Analog 7

Many applications, as in power supply modules and automotive, need to know when the system reaches some critical temperature. The LM26 and LM27 provide a single output which goes active when the temperature crosses the trip-point of the device. This output can, for example, be read by a system processor as an alarm signal or be used to turn on a fan to start cooling down the system.

Additionally, the LM26 and LM27 feature an analog temperature output. This V_{TEMP} output provides a voltage that is proportional to the measured temperature. The V_{TEMP} pin can also be used for production system testing. Driving the V_{TEMP} pin to ground will force the output to trip, and the system can read the $\overline{OS}$ output to verify functionality.

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The Sight & Sound of Information

Thermal Management: Remote Diode Temperature Sensors (RDTS)

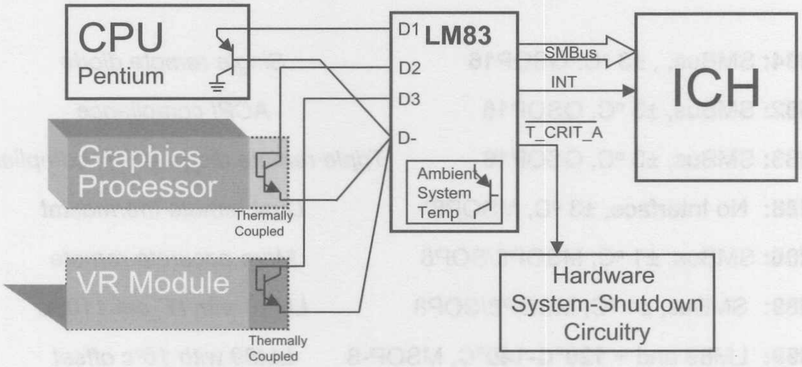
Remote Diode Temperature Sensor (RDTS) ICs normally measure the temperature of a thermal diode inside of a large chip, such as a Pentium® processor or an FPGA. That diode temperature is then compared to certain temperature thresholds and output signals are generated based upon these comparisons. RDTS ICs also have an internal thermal diode that is used to measure the local temperature of the IC itself. The output of the RDTS can also be based upon the local temperature as compared to fixed temperature threshold settings.

Remote Diode Temperature Sensors

LM84: SMBus, , ±3 °C, QSOP16	*Single remote diode*
LM82: SMBus, ±3 °C, QSOP16	*ACPI compliance*
LM83: SMBus, ±3 °C, QSOP16	*Triple remote diode, ACPI compliance*
LM88: No Interface, ±3 °C, MSOP8*	*Dual remote thermostat*
LM86: SMBus, ±1 °C, MSOP8/SOP8	*More accurate remote*
LM89: SMBus, ±1 °C, MSOP8/SOP8	*LM86 with tT_crit 110 °c*
LM99: LM89 and + **120°C-140°C,** MSOP-8	*LM89 with 16°c offset*
LM90: ± 3 °C version of LM86	*Smallest package 3 °c*
LM63: SMBus, ±1 °C, **Fan Control**, SO-8	*Small, low cost, 1°C, programmable* ***fan control***

National Semiconductor's line of remote diode temperature sensors differ from analog, digital and thermostat products in that they have the ability to measure remote temperatures, not just their local temperature. RDTSs differ from hardware monitors in that they are simpler devices without system monitoring inputs and multiple outputs. National Semiconductor offers a wide variety of RDTSs with different accuracies, numbers of inputs, interfaces, and output signals. The following slides will go into each of the parts in more detail.

Typical RDTS Application



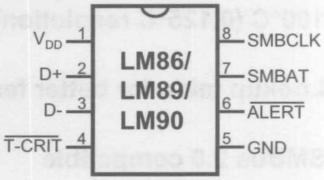
- **RDTS resolves placement issues**
- **Thermally-coupled diode-connected 2N3904's are used in non CPU locations**

The multipoint RDTS LM83 directly senses its own temperature and the temperature of three external PN junctions, or diodes. One may be dedicated to the CPU while the other two may be dedicated to another part of your system that may have an overheating issue, such as the disk drive and graphics processor. By monitoring the temperature of a specific area, the overall temperature in the box is given more room to move.

The LM83 supports I^{2}C Bus and SMBus interfaces. It has user-programmable limits and WATCHDOG capability with Interrupt output as well as a critical temperature alarm output for system power supply shutdown.

LM86, LM89 ± 1°C and LM90 ± 3°C Remote Diode Temperature Sensors

- **Newest family of CMOS7 process RDTS's**
- 0.125°C remote resolution
- SMBus 2.0 compatible
- Remote + local temperatures
- User-Programmable digital filter
- ALERT and T_Crit open-drain outputs
- Tiny MSOP-8 or SO-8 package



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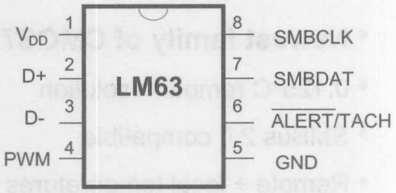
The Art of Analog II

In today's world, electronics systems are running faster and getting hotter. Large components can get so hot that they destroy themselves or damage circuitry around them. Let's take network motherboards for example. If the CPU chip gets hot it may be necessary to "throttle-back" on the speed to allow the system to keep running, but at a diminished capacity. The ALERT function of the LM86 can be used to trigger the "throttle-back" circuitry. If, however, the CPU chip exceeds a maximum temperature limit, the output of the LM86 can trigger the system's shutdown circuitry. This protects the board circuitry from heat damage and signals the system that something is getting unbearably hot and is shutting down.

LM63: ±1 °C RDTS & Fan Control



- **RDTS controls fan output**
- **±1°C remote accuracy from 60°C to 100°C (0.125°C resolution)**
- **Lookup table for better fan acoustics**
- **SMBus 2.0 compatible**
- **Multi-function pin 6: ALERT or TACH**
- **SO-8 package**

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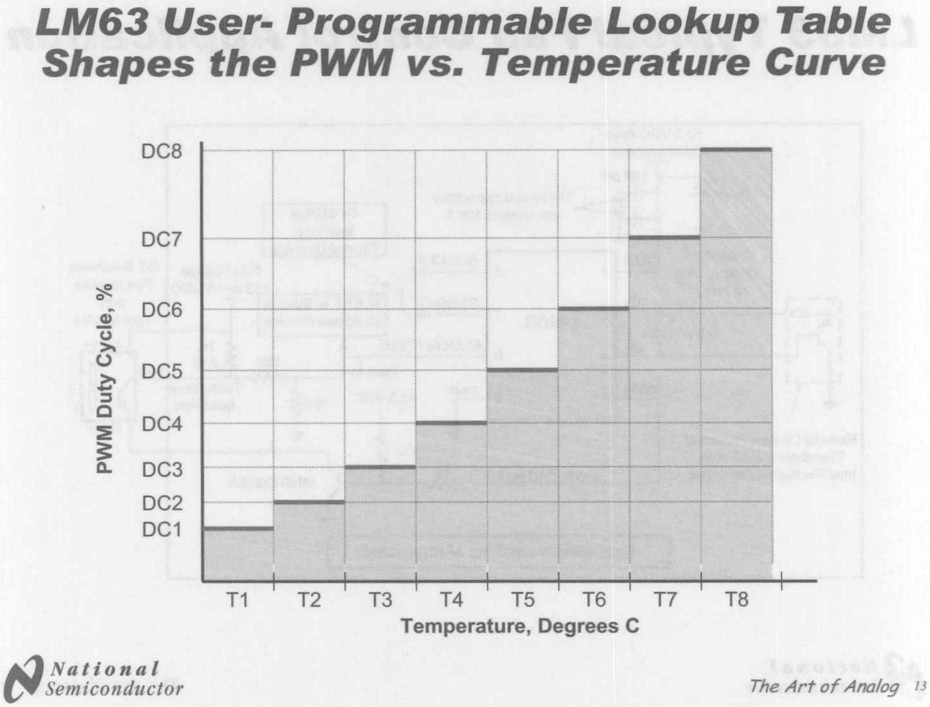
The Art of Analog 12

Microprocessors, FPGAs and voltage regulator modules are just a few examples of heat generators commonly found on today's circuit boards. Fans are often employed to blow cool air across heat sinks attached to the chips or to circuit boards. The new LM63 is National's high accuracy remote diode temperature sensor with sophisticated fan control output. An RDTS measures the voltage across a PN junction at two different current levels and calculates the temperature based upon these readings. National Semiconductor's LM63 can measure device temperature and provide an appropriate fan speed control signal to cool the device or system to a desired level.



LM63 User- Programmable Lookup Table Shapes the PWM vs. Temperature Curve

National Semiconductor

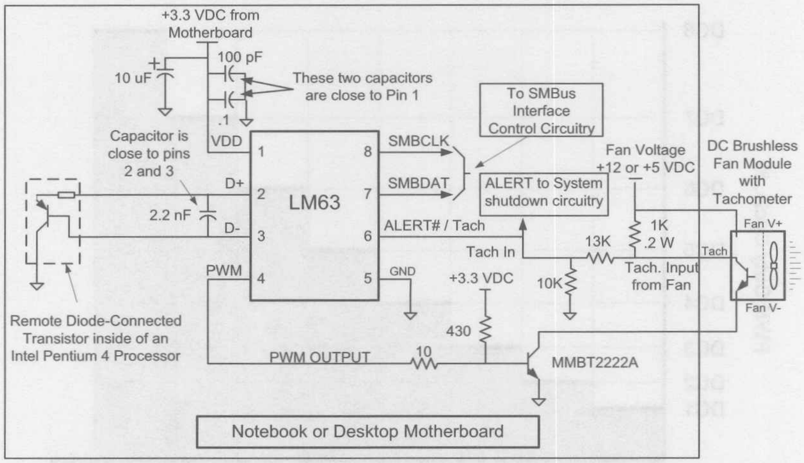
The Art of Analog 13

The LM63 generates an energy-efficient PWM signal to control the fan speed. One of the problems with fan speed control is the irritating audible fan noise as it cycles on and off, speeding up or slowing down. National Semiconductor's LM63 is the first RDTS on the market that has a user-programmable Lookup Table so that the user can shape the output signal for minimum fan noise!

The LM63 has over 30 selectable drive frequencies. The duty cycle is determined by the remote diode temperature. As the temperature increases, the duty cycle is changed to increase the fan speed. As the temperature decreases, the PWM duty cycle decreases. Hysteresis is used to help prevent the fan from oscillating between two temperature measurements. Also incorporated into this PWM lookup table is a fan start-up routine. When the temperature is greater than the first table entry, the fan goes though a start-up routine to overcome stationary inertia.

The Duty Cycle/Temperature (DCx/Tx) pairs are user programmed.

LM63 Typical Fan Control Application

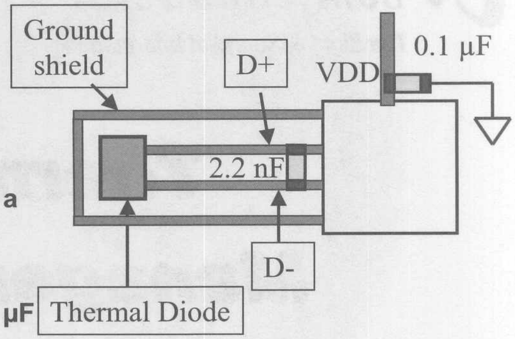

+3.3 VDC from Motherboard
100 pF
10 uF
These two capacitors are close to Pin 1
.1
To SMBus Interface Control Circuitry
Capacitor is close to pins 2 and 3
VDC
1
8
SMBCLK
D+
2
LM63
7
SMBDAT
ALERT to System shutdown circuitry
Fan Voltage +12 or +5 VDC
DC Brushless Fan Module with Tachometer
2.2 nF
D-
3
6
ALERT# / Tach
1K
.2 W
Fan V+
Tach In
13K
Tach
PWM
4
5
GND
+3.3 VDC
10K
Tach. Input from Fan
Fan V-
Remote Diode-Connected Transistor inside of an Intel Pentium 4 Processor
430
PWM OUTPUT
10
MMBT2222A
Notebook or Desktop Motherboard

The PWM signal generated by the LM63 can be used to control the fan speed through a bipolar transistor or FET.

If the user has a fan with a tachometer output, the ALERT#/TACH pin can be programmed to accept this tachometer signal and measure the RPM of the fan as confirmation that the fan is, indeed, running. With the LM63 the user can now have both a cool and a quiet system. The LM63's combination of a single remote diode input, a single PWM fan control output and one degree Celsius accuracy makes this a unique product.

PCB Layout Suggestions to Reduce Noise

- **Diode traces short, wide, parallel, and away from switching signals.**
- **Diode traces encircled with a ground shield, if possible**
- **VCC line bypassed with 0.1 µF capacitor**



For the best chance of success in your system you need to follow PC board layout guidelines that will minimize the risk of noise-caused erroneous readings. Shown here is a summary of layout considerations to watch out for.

Keep the traces to the thermal diode as short as possible, parallel, and as wide as practical for minimum resistance. The diode traces should be placed away from high-speed switching lines and, ideally, encircled with a shielding loop. National Semiconductor recommends avoiding power supply switching inductors and placing the 2.2 nF capacitors as close to the device as possible. The VDD line should have a 0.1 microfarad capacitor as close to the VDD lead as possible.

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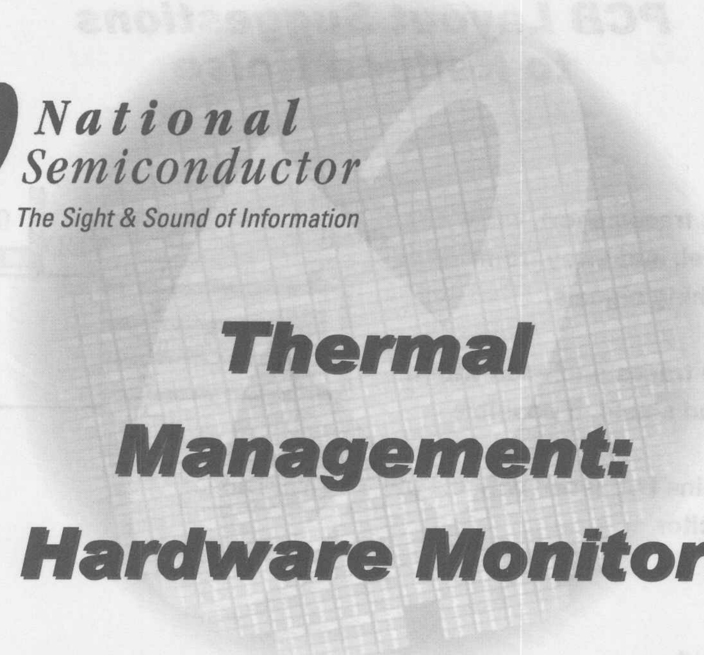
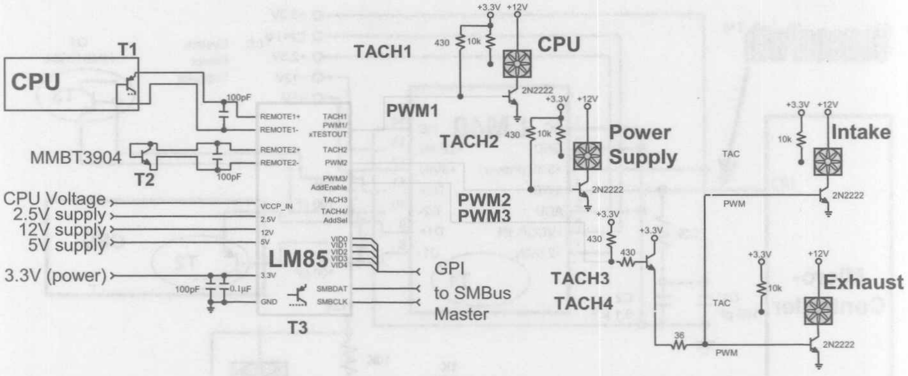


Thermal Management: Hardware Monitors

Monitor and Control Up to Four Fans



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The Art of Analog 17

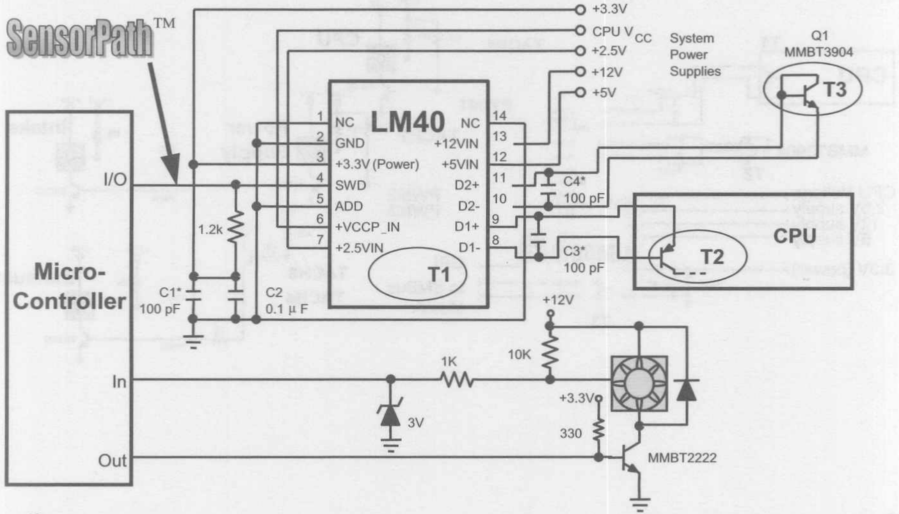
Monitor and control of up to four fans are possible using the LM85 hardware monitor. Fans are being included in more and more systems lately and the noise they produce can be reduced through thermal monitoring of critical system nodes and adjusting the fan speed to accommodate the variation in the measured temperature. Systems are usually designed for a maximum ambient temperature that is rarely achieved, so why run the fans full on when not necessary?

The LM85 has fully autonomous fan speed control. Three PWM open-drain outputs are available to control three or more fans. Signal conditioning can be added to the LM85 PWM outputs to provide DC drive, high side PWM drive or low side PWM drive for fan power as shown here. Each of the PWM outputs can drive multiple fans, as shown on PWM3 here.

Three thermal zones can be accommodated as shown here: the temperature sensed by the LM85 junction temperature (T3) and two remote diode temperature sensor inputs that can monitor, for example, the thermal diode of a processor or ASIC (T1) as well as an MMBT3904 diode-connected transistor (T2).

The serial interface for the LM85 is simply comprised of 2 control lines SMBDAT and SMBCLK that are compatible with SMBus 2.0. No interrupt is required since the LM85 fan control registers enable full autonomous fan control. Internal scaling resistors are provided to monitor system power supply voltages (3.3V, 5V, 12V, 2.5V) and processor core voltage. Four 16-bit counters monitor the speed of 4 fans. In some processors the core voltage is a function of the setting of the processors VID pins, so there are five logic inputs to monitor the state of VID0-VID4. These pins can also be used as general purpose digital inputs as well.

LM40 Flexible System Fan Control with Voltage Monitoring



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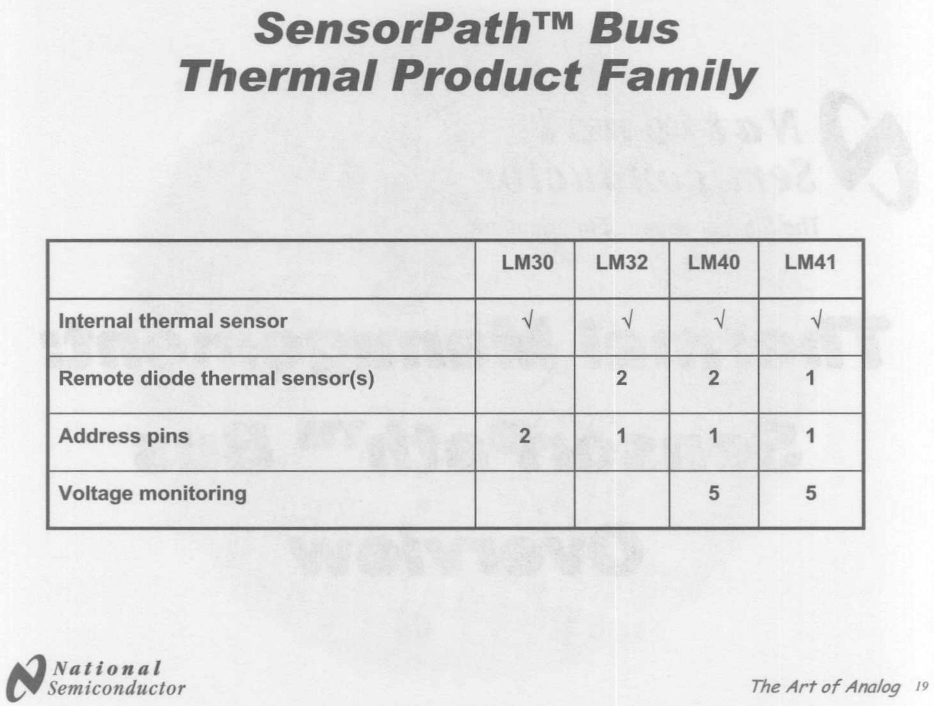
* Note, place close to LM40 pins.

The Art of Analog 18

Shown here is a flexible system with fan control and voltage monitoring. The LM40 is connected to the micro-controller via a single wire interface called SensorPath™, which has just been introduced by National Semiconductor. The LM40 monitors 5 voltage inputs and 3 thermal zones (T1-T3), similar to the LM85. The micro-controller in turn monitors the fan tachometer output signal and drive a PWM output to control the fans speed with the MMBT2222.

SensorPath™ has been specifically designed and optimized for sensor devices. Using SensorPath™, theoretically up to 7 devices such as the LM40 can be placed on one wire. This would allow up to 28 thermal zones to be analyzed and used to adjust the speed of one fan. It is highly unlikely that there will ever be a need for 7 devices to be connected on one such Bus, but it is used to show the flexibility of SensorPath™.

The LM40 includes internal scaling resistors for voltage monitoring.



SensorPath™ Bus Thermal Product Family

	LM30	LM32	LM40	LM41
Internal thermal sensor	√	√	√	√
Remote diode thermal sensor(s)		2	2	1
Address pins	2	1	1	1
Voltage monitoring			5	5

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The Art of Analog 19

National Semiconductor will release a whole family of products that will support the SensorPath bus. The first being the LM30 followed by the simultaneous release of the LM32, LM40 and LM41 devices. We have just discussed the LM40. The other 3 devices are a sub-set of the LM40. To simplify this table, only the product functions are discussed here. In the appendix you will find details on the key specifications of these devices as well as pinout and block diagram information.

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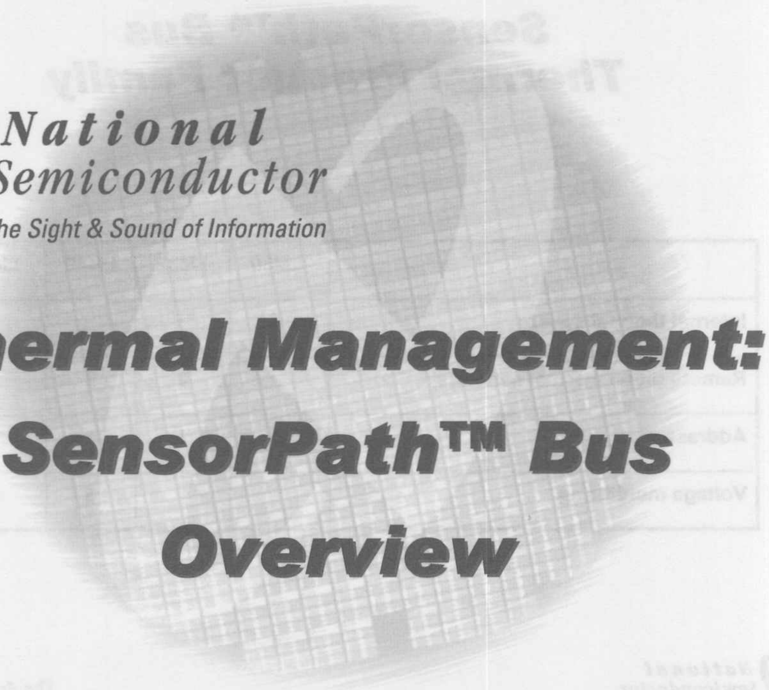


Thermal Management: SensorPath™ Bus Overview

This overview covers the basics of the SensorPath™ bus. SensorPath is specifically targeted for sensors, allowing for a very simple definition. We will discuss the physical, bit, and message layers of the bus. The SensorPath specification also includes a programming model for different types of functions including, but not limited to, voltage, temperature, and EEPROM. The programming model will not be covered here in detail, but information can be found on any of the released product datasheets.

It is not customary to add a programming model to a "Bus" specification. Doing so for software "simple" devices such as voltage and temperature sensors allows device-to-device compatibility without requiring firmware changes while providing system scalability.

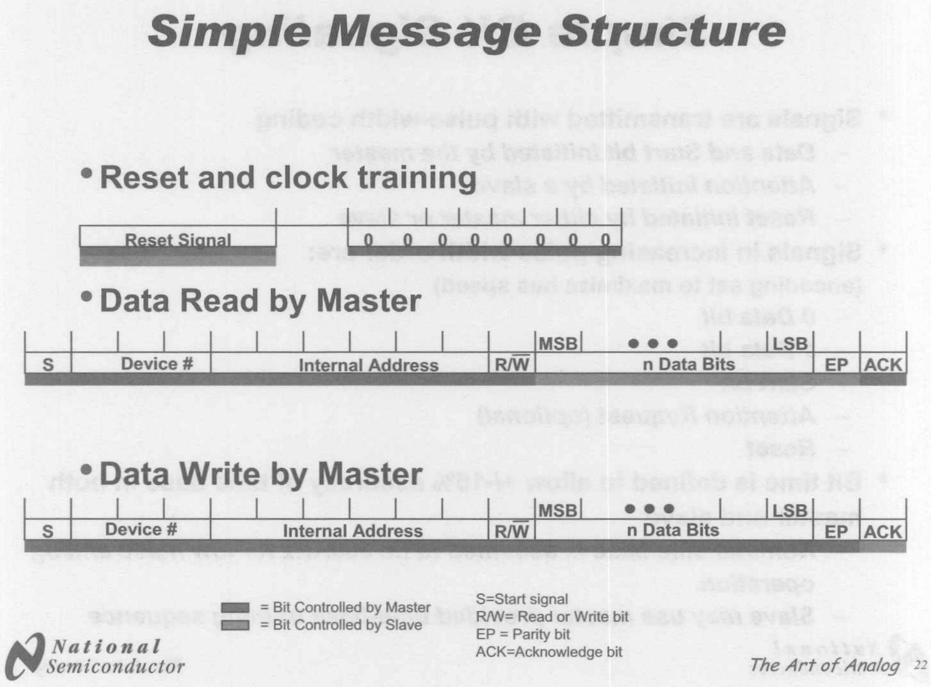
Simple Bit Signaling

- **Signals are transmitted with pulse-width coding**
  - ***Data and Start bit initiated by the master***
  - ***Attention initiated by a slave***
  - ***Reset initiated by either master or slave***
- **Signals in increasing pulse-width order are:**
  (encoding set to maximize bus speed)
  - ***0 Data bit***
  - ***1 Data bit***
  - ***Start bit***
  - ***Attention Request (optional)***
  - ***Reset***
- **Bit time is defined to allow +/-15% accuracy of time base in both master and slave**
  - ***Nominal time base is assumed to be 360KHz for low noise analog operation.***
  - ***Slave may use master provided time-base training sequence***

The SensorPath™ signaling is very simple. The physical layer of SensorPath is the same as the SMBus SMBDAT signal. It is an open-drain bi-direction input/output that can drive a 0.4V logic low with 4 mA output current with a maximum load capacitance is 400 pF. Bits are signaled using various pulse widths.

There are 5 different signals: 0 bit, 1 bit, Start Bit, Attention Request and Reset. The signals are encoded in order to maximize the bus bandwidth. The Data and Start bits are initiated by the master, Attention is initiated by the slaves and Reset can be initiated by either the master or the slave. A signal is initiated on the bus by a high to low transition. An attention may be transmitted in the middle of a transaction or when the bus is idle.

Since the slaves may have analog functions sensitive to high frequency noise, a fairly slow time base of 360 kHz has be used to set the pulse-width of the different signals. The tolerance of this time base for the master and slave(s) is +/-15%. The pulse width tolerance of the signals have been set to accommodate this overall skew between the master and slave of 30% maximum and the physical layer limitations of 4mA logic low drive strength with a 400 pF bus capacitance. After the Reset signal the master will transmit a time-base training sequence. The slave may use this sequence to adjust the pulse width of its output signals. This may be necessary if the +/-15% clock tolerance is not achievable in the slave device. It is not mandatory for all slaves to support clock training. Therefore time base training cannot be used to change the time base of the slaves to something other than 360 kHz.



Simple Message Structure

- Reset and clock training

Reset Signal	0	0	0	0	0	0	0	0

- Data Read by Master

S	Device #	Internal Address	$R/\overline{W}$	MSB ● ● ● LSB n Data Bits	EP	ACK

- Data Write by Master

S	Device #	Internal Address	$R/\overline{W}$	MSB ● ● ● LSB n Data Bits	EP	ACK

▆ = Bit Controlled by Master
▆ = Bit Controlled by Slave

S=Start signal
R/W= Read or Write bit
EP = Parity bit
ACK=Acknowledge bit

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The Art of Analog 22

The message structure of SensorPath™ is also simple. There are three different messages that can be transmitted: Reset and clock training, Data Read by Master, and Data Write by Master. Reset and clock training is the simplest. After power on the master and slaves must drive a reset signal.

Data read and write by Master are very similar transactions. The difference being which device (master or slave) actually controls the Data, EP and ACK bits. The Start signal initiates a transaction and is transmitted by the master. The master then transmits the 3-bit device address. Up to 7 devices can be accommodated on one line. If more devices are required, other bus nodes will have to be supported by the Master. The master then transmits the slave device internal 6-bit address followed by the Read/Write# bit. The rest of the Data Read and Write by Master transactions continue like so:

If the transaction is a Read by Master the slave will transmit the data bits. The slave then determines the parity of the transaction and then transmits the EP bit. The master acknowledges the state of EP bit by transmitting an ACK.

If the transaction is a Write by Master the master will transmit the data bits. The master then determines the parity of the transaction and then transmits the EP bit. The slave acknowledges the state of the EP bit by transmitting an ACK.

Micro-Controller Programming Hints: Bit Pulse Detection

- High to low SensorPath™ Bus edge interrupt
  - *Starts pulse timer*
- Low to high SensorPath™ Bus edge interrupt
  - *Stops pulse timer*
  - *Determines bit type from the time*
  - *If attention bit, sets attention flag*

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The Art of Analog 23

A simple method to detect the input bit is to have interrupts on the falling and rising edges. The length of the pulse determines its bit type. If an attention bit occurs, it is noted.

Micro-Controller Programming Hints: Alternative bit pulse detections

If edge interrupts are not available, alternatives are:

- *Use low/high level interrupts to detect edges*
- *Use timers which count on low/high only and overflow on an edge*
- *Use microcontroller support (if any) for direct pulse width detection*
- *Poll the bus (least desirable)*

There are several alternative ways to detect the pulse width. The edge level interrupts can be replaced by low/high level interrupts. Timers which count on only high or low levels can be used to detect each edge also. The microcontroller hardware may directly support pulse width detection. The last resort is to poll the bus which is least desirable as it is processor intensive.

Micro-Controller Programming Hints: Bit Output Pulse Generation

- Start an output timer and drive bus low. When timer overflow interrupt occurs, release bus
- An alternative is to drive the bus low and watch for the read bit pulse timer to count to the desired value
- Another alternative is to use the microcontroller support (if any) for direct pulse generation

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To generate the output bit pulse of the desired length, an output timer can be started when the bus is driven low. The timer interrupt will occur when the time expires, and the bus is then released. An alternative if a second timer is not available is to drive the bus low, and watch the read bit pulse timer count to a desired value. Optionally, the microcontroller may directly support pulse generation.

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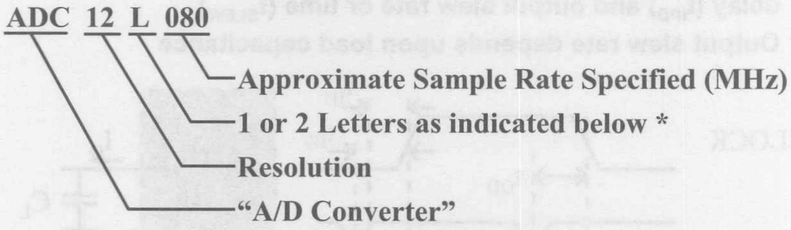
Analog-to-Digital Converter Application Techniques

Analog-to-digital converters are conceptually simple: give them an analog voltage (or current) and they give you a digital word. Applying ADCs, however, is not quite so trivial. Past seminars have focused on many areas to ease the ADC design task and maximize ADC performance. Here we discuss some ways to ease the use of these products

Nomenclature for National Semiconductors High Speed ADCs


ADC 12 L 080
Approximate Sample Rate Specified (MHz)
1 or 2 Letters as indicated below *
Resolution
"A/D Converter"

* D – Dual
L – Low Voltage (3.3V or less)
Q – Quad
S – Serial (LVDS) Outputs
T – Triple

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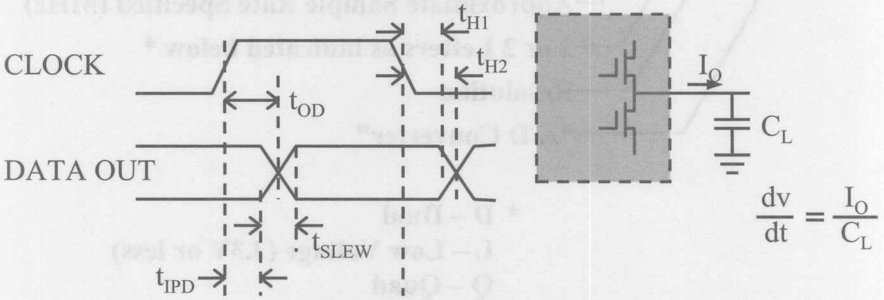
While there are some exceptions to this method of specifying our products, this method generally holds for newer devices. The letters following the resolution may be combined, as in the cases of the ADC12DL066, which is a dual, low voltage, 12-bit, 66 MSPS ADC.
At this time we do not have any quads or triples being offered, but they are planned.

Output Timing

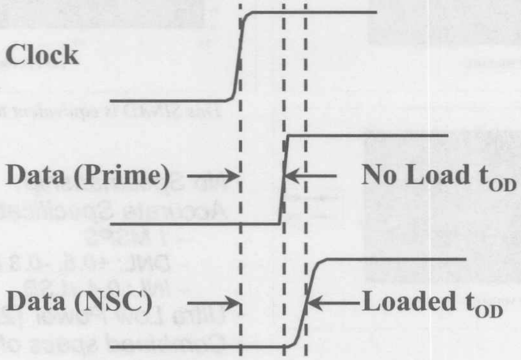
- Output Delay (t_{OD}) and hold (t_{H1}, t_{H2}) times depend upon internal delay (t_{IPD}) and output slew rate or time (t_{SLEW})
- Output slew rate depends upon load capacitance



ADC timing specifications can be critical and should be used like any digital timing specification. Output delay and hold times tell us the data transition points relative to a reference signal. These times should be compared with setup and hold times of the digital data receiver. Output delay and hold times consist of an internal delay plus some part of the output signal rise and/or fall times. Since the output drivers of the ADC have a finite current capability, the rise and fall times of the output signals will depend upon the load capacitance. As we increase the capacitance at the output we increase the delay and hold times.

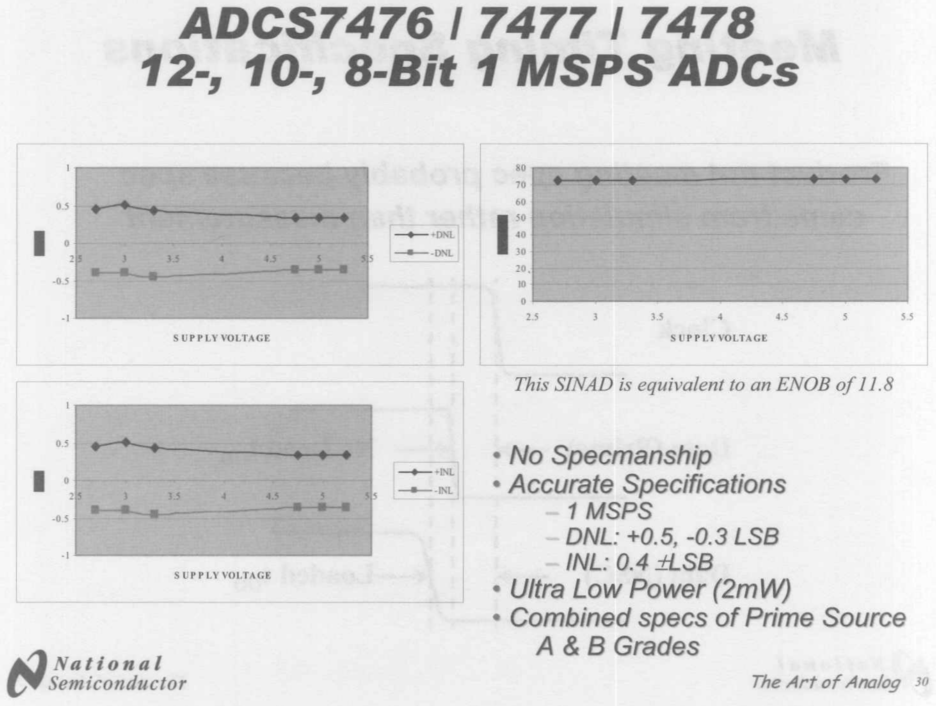
Meeting Timing Specifications

Product not meeting spec probably because spec came from simulation rather than measurement



We have found that some competitive products do not meet their own timing specifications! An analysis of the situation reveals that there must be no load at the output to realize the timing claimed on the data sheet. We have concluded that the manufacturer most likely simulated the timing and neglected to provide a load in the simulation.

Bob Pease is vindicated! It is important to verify all simulations with actual measurements.


1
0.5
0
-0.5
-1
2.5
3
3.5
4
4.5
5
5.5
+DNL
-DNL
SUPPLY VOLTAGE
80
70
60
50
40
30
20
10
0
2.5
3
3.5
4
4.5
5
5.5
SUPPLY VOLTAGE
1
0.5
0
-0.5
-1
2.5
3
3.5
4
4.5
5
5.5
+INL
-INL
SUPPLY VOLTAGE

ADCS7476 / 7477 / 7478
12-, 10-, 8-Bit 1 MSPS ADCs

This SINAD is equivalent to an ENOB of 11.8

- *No Specmanship*
- *Accurate Specifications*
  - *1 MSPS*
  - *DNL: +0.5, -0.3 LSB*
  - *INL: 0.4 ±LSB*
- *Ultra Low Power (2mW)*
- *Combined specs of Prime Source A & B Grades*

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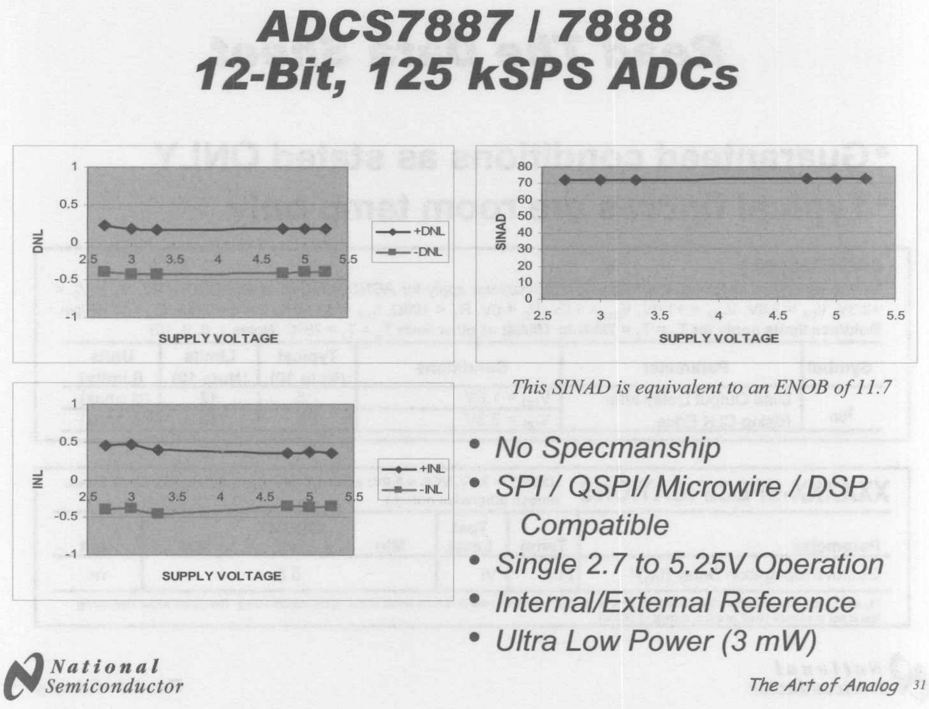
The Art of Analog 30

It is the prime original source of these products that we found did not meet their own timing specs until we completely removed the load. Practical circuits must have loads. The timing specs may have come from simulations and the manufacturer might have forgotten to simulate with a load.

When you compare our specifications with those of the prime source of these products, you will see a difference because our specs are for practical loads.



ADCS7887 / 7888
12-Bit, 125 kSPS ADCs

This SINAD is equivalent to an ENOB of 11.7

- *No Specmanship*
- *SPI / QSPI/ Microwire / DSP Compatible*
- *Single 2.7 to 5.25V Operation*
- *Internal/External Reference*
- *Ultra Low Power (3 mW)*

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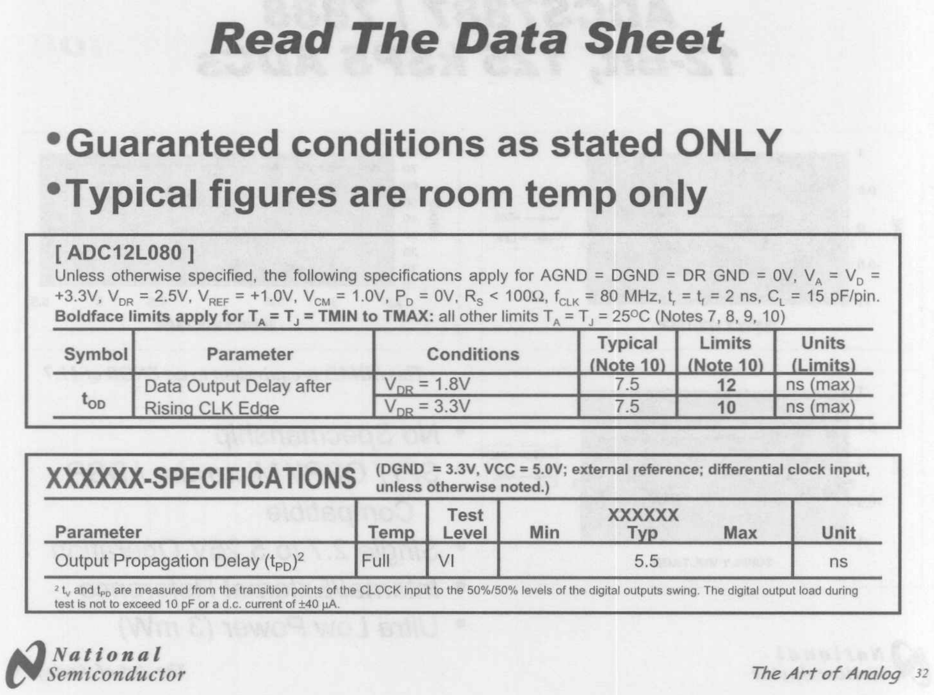
The Art of Analog 31

These products are also new alternate source ADCs for the general purpose market. Again, you will find that ours are completely and clearly specified.



Read The Data Sheet

- Guaranteed conditions as stated ONLY
- Typical figures are room temp only

[ADC12L080]

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D$ = +3.3V, V_{DR} = 2.5V, V_{REF} = +1.0V, V_{CM} = 1.0V, P_D = 0V, $R_S < 100\Omega$, f_{CLK} = 80 MHz, $t_r = t_f$ = 2 ns, C_L = 15 pF/pin. **Boldface limits apply for $T_A = T_J$ = TMIN to TMAX:** all other limits $T_A = T_J$ = 25°C (Notes 7, 8, 9, 10)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
t_{OD}	Data Output Delay after Rising CLK Edge	V_{DR} = 1.8V	7.5	**12**	ns (max)
		V_{DR} = 3.3V	7.5	**10**	ns (max)

XXXXXX-SPECIFICATIONS **(DGND = 3.3V, VCC = 5.0V; external reference; differential clock input, unless otherwise noted.)**

Parameter	Temp	Test Level	Min	XXXXXX Typ	Max	Unit
Output Propagation Delay (t_{PD})[2]	Full	VI		5.5		ns

[2] t_V and t_{PD} are measured from the transition points of the CLOCK input to the 50%/50% levels of the digital outputs swing. The digital output load during test is not to exceed 10 pF or a d.c. current of ±40 μA.

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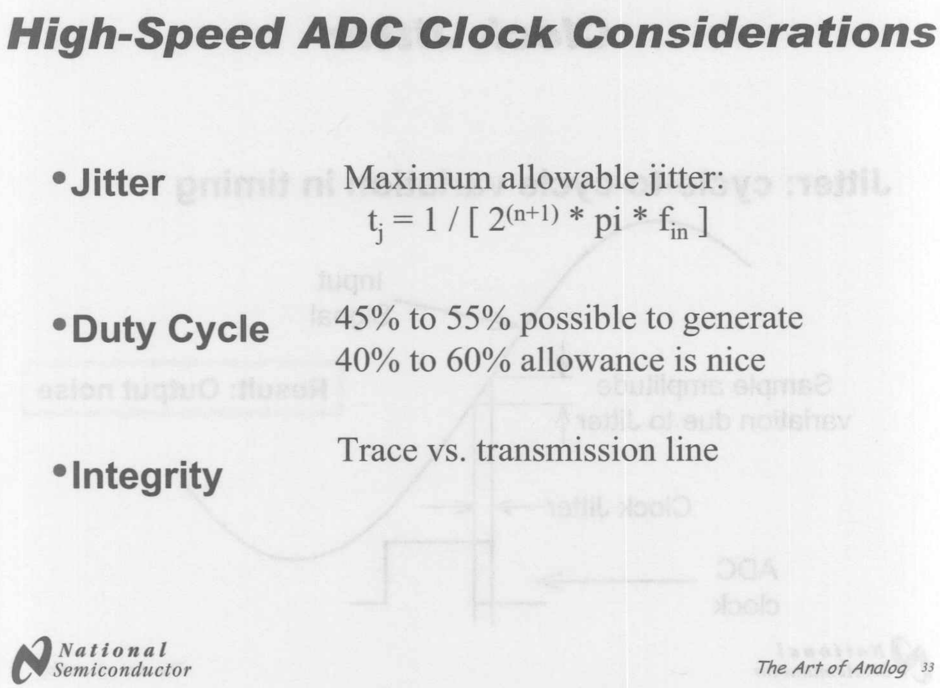
The Art of Analog 32

We have seen a lot of problems because some customers have not paid attention to the specifications. One problem is not reading the data sheet and understanding that the typical figures are room temperature only and that they offer not guarantees. Note that the upper spec shown here indicates that t_{PD} is constant with temperature. This is highly questionable. The upper specification indicates a maximum delay over the entire temperature range with the typical case listed for room temperature. The t_{OD} of the upper spec is equivalent to the t_{PD} of the lower spec.

Note the upper specification is more complete than the lower one. It specifies the reference voltage, clock rate, clock rise and fall times and the state of digital control pins. These specifications may not be important for all tests and not all of them are important for the one test shown here.

The upper specification is from the preliminary version of the ADC12L080 data sheet.



High-Speed ADC Clock Considerations

- **Jitter** Maximum allowable jitter: $t_j = 1 / [\ 2^{(n+1)} * pi * f_{in}\ ]$
- **Duty Cycle** 45% to 55% possible to generate; 40% to 60% allowance is nice
- **Integrity** Trace vs. transmission line

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The Art of Analog 33

Jitter can be described as the cycle-to-cycle variation in the period of a waveform. Jitter in the sampling clock or in the input waveform (actually, the jitter between the two) results in decreased noise performance, as we will see shortly. The maximum jitter, for all sources, is as shown here if we are to prevent it from affecting performance. Jitter is a prime source of noise with high frequency signals. Note that neither sample rate not signal amplitude enter this formula.

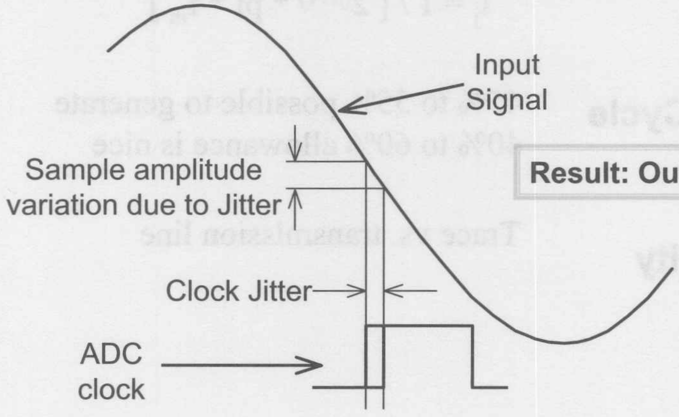
Most people use a 2n factor, but this limits the noise to one LSB. Using a factor of 2(n+1), as shown here, limits the noise to ½ LSB, which means, for all practical purposes, no noise.

It is difficult to generate a clock signal with exactly 50% duty cycle, but it is possible to produce duty cycles of 45% to 55%. Products that work well with 40% to 50% duty cycles can ease the design task.

All lines are transmission lines, even though we can generally treat very short lines as simple connections.

Clock Jitter

Jitter: cycle-to-cycle variation in timing

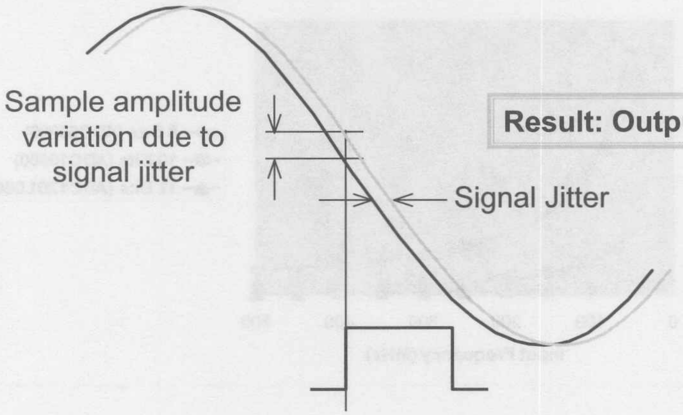


Result: Output noise

Because jitter in the ADC clock relative to the input signal means that there is a variation in the time a signal is sampled, there is variation in the sampled signal level. That is, if we try to sample the same point in a waveform at every cycle of that waveform, but there is jitter present, we may sample levels between, say 1.14V to 1.15V, or a 10 mV spread. This means there is 10 mV of noise at the output. At 6 or 8 bits resolutions this might not be too bad. But at higher resolutions this can be significant.

Signal Jitter

Signal jitter has the same effect as clock jitter



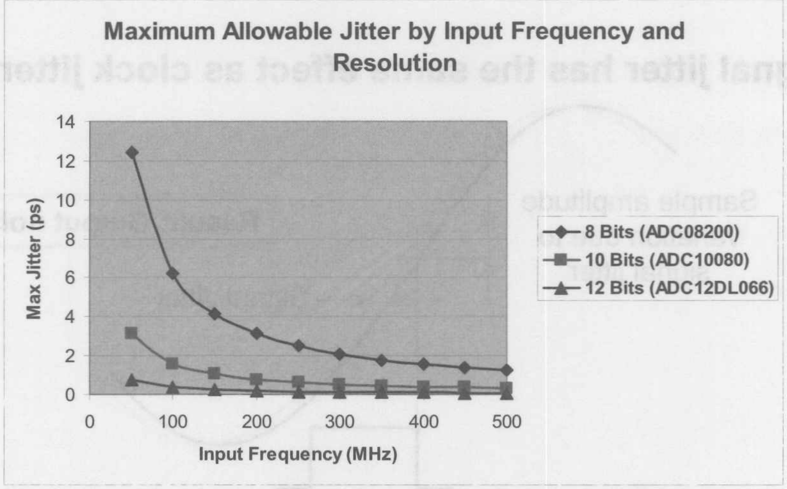
Sample amplitude variation due to signal jitter

Signal Jitter

Result: Output noise

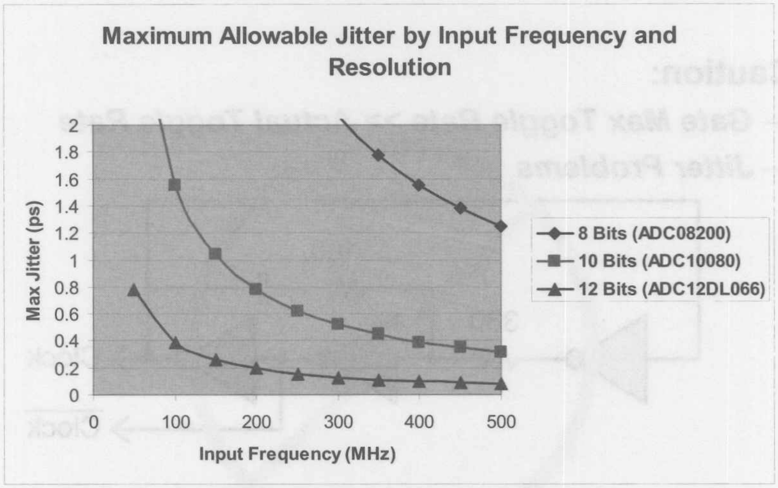
Jitter in the input signal has the same effect as does jitter in the sample clock. The clock jitter relative to the signal jitter is where the problem lies.

Maximum Jitter



The maximum jitter tolerable without suffering a degradation in SNR is determined by the resolution of the A/D Converter and the frequency of the input signal. Again, neither the amplitude of the signal nor the sample rate has any effect.

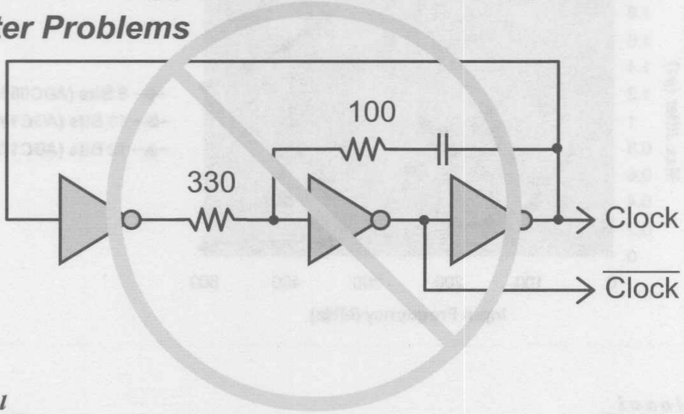
Maximum Jitter(2)



This is the same as the previous slide with the vertical scale expanded.
It seems that avoiding noise induced jitter is an impossible task at very high input frequencies and high resolutions. Careful selection of the the clock source and how it is presented to the ADC, as well as proper attention to design and layout, will go a long way to maximizing circuit performance.

How NOT to Generate A High-Speed ADC Clock - Gates

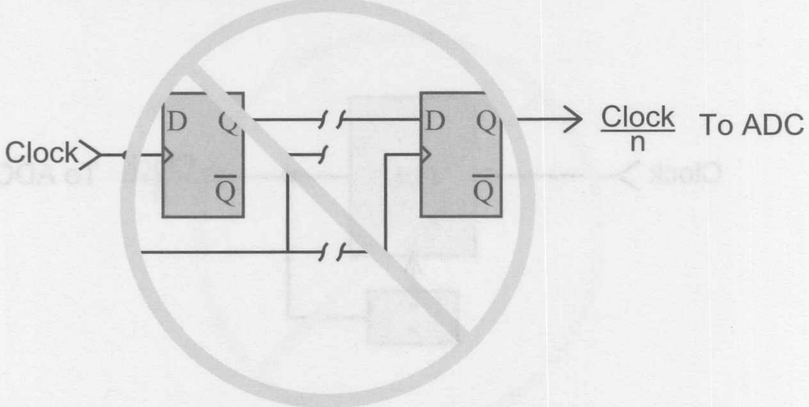
- **Caution:**
  - ***Gate Max Toggle Rate >> Actual Toggle Rate***
  - ***Jitter Problems***



Generating a high speed clock with simple gates will produce excessive jitter unless the actual toggle rate of the gates is significantly less than their maximum capability.

How NOT to Generate A High-Speed ADC Clock - Dividers

- Same Cautions as With Gates
- More Stages Means More Jitter



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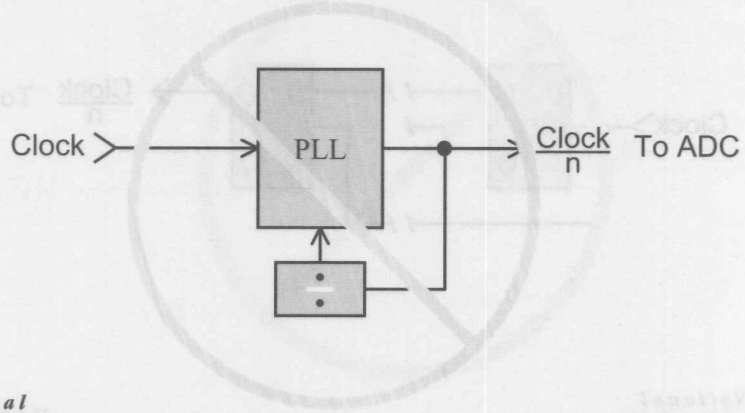
Dividers have the same jitter problem as do simple gates.

How NOT to Generate A High Speed ADC Clock - PLLs

PLLs are notorious for creating jitter



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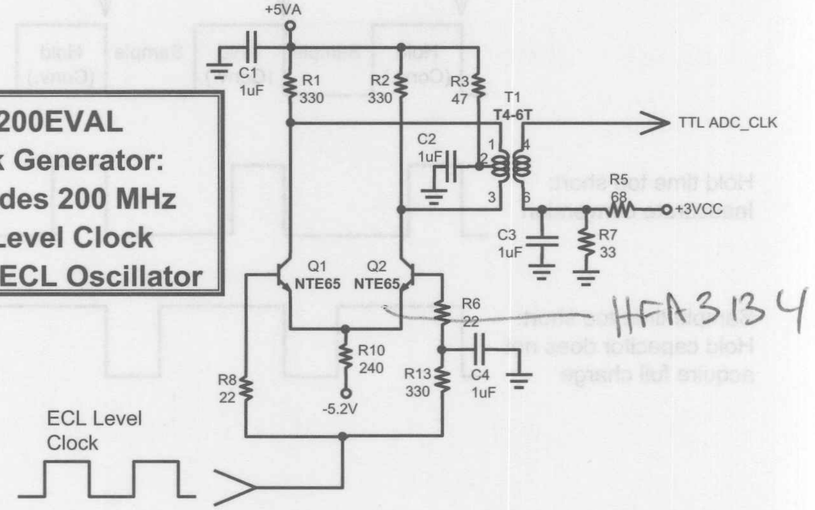
Need we say more?.

Generating A High-Speed Clock



HFA3134

ADC08200EVAL
Clock Generator:
Provides 200 MHz
TTL-Level Clock
from ECL Oscillator

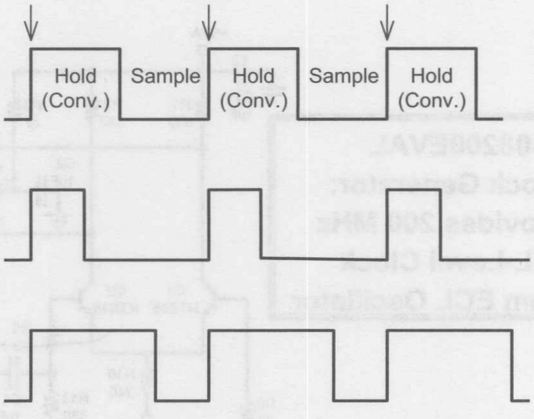
National Semiconductor

The Art of Analog 41

This circuit is used on our ADC08200 evaluation board. The ADC08200 needs a TTL-level clock but common oscillators at very high frequencies are not available with TTL outputs. However, Pletronics (http://www.Pletronics.com), and possibly other oscillator manufacturers, will build such an oscillator if the quantity is sufficient.

We have found that NTE65 substitutes from manufacturers other than NTE Electronics may not have sufficient gain for this circuit.

Clock Duty Cycle



Hold time too short:
Inaccurate conversion

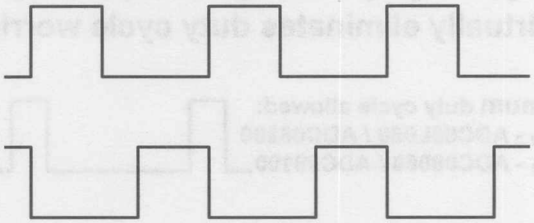
Sample time too short:
Hold capacitor does not
acquire full charge

The duty cycle of the clock used for high speed ADCs can be critical. If the Sample-and-Hold amplifier at the ADC front end is in the “hold” mode with the clock is high and the “sample” mode when it is low, as shown here, a short duty cycle might not hold the signal long enough for conversion. If the duty cycle is too long, the sample time is too short and the signal might not be adequately acquired.

Either of these cases can cause erroneous conversions. The extreme case would be a complete failure of the ADC to function.

Clock Duty Cycle Allowed by Some ADCs

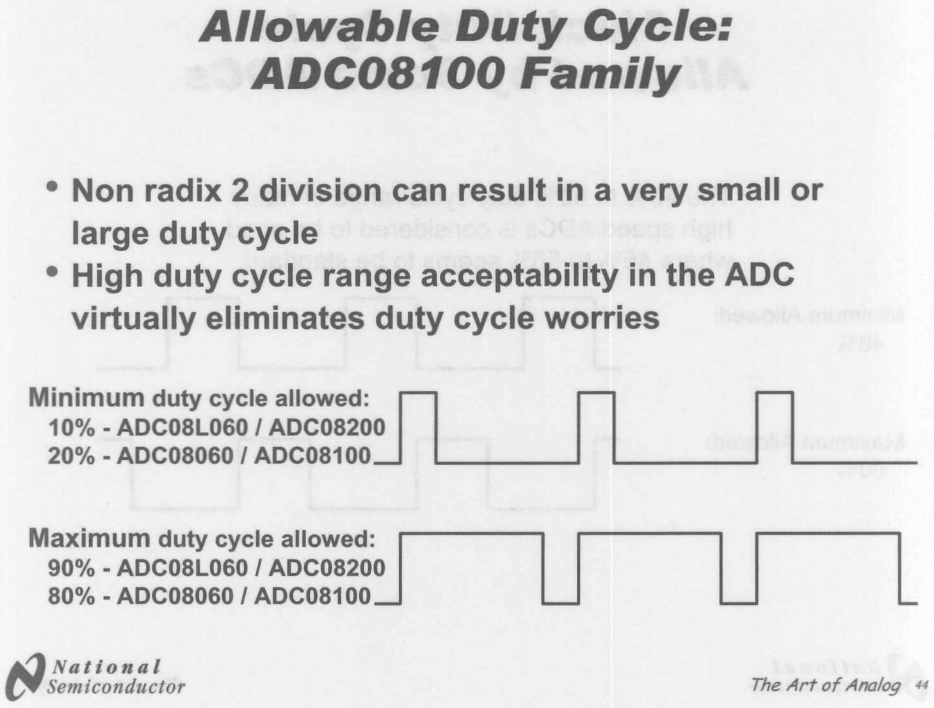
The 40% to 60% duty cycle range of many high speed ADCs is considered to be good, where 45% to 55% seems to be standard.



Minimum Allowed:
40%

Maximum Allowed:
60%

Developing a clock signal with duty cycles of 45% to 55% is certainly a task that is not too difficult. Tighter duty cycle limits, however, could be a problem. Canned oscillators generally have 45% to 55% duty cycle limits, so an ADC should be able to adequately perform over this duty cycle range. Many ADCs today perform well over duty cycles of 40% to 50% and more.



Allowable Duty Cycle: ADC08100 Family

- **Non radix 2 division can result in a very small or large duty cycle**
- **High duty cycle range acceptability in the ADC virtually eliminates duty cycle worries**

Minimum duty cycle allowed:
10% - ADC08L060 / ADC08200
20% - ADC08060 / ADC08100

Maximum duty cycle allowed:
90% - ADC08L060 / ADC08200
80% - ADC08060 / ADC08100

National Semiconductor

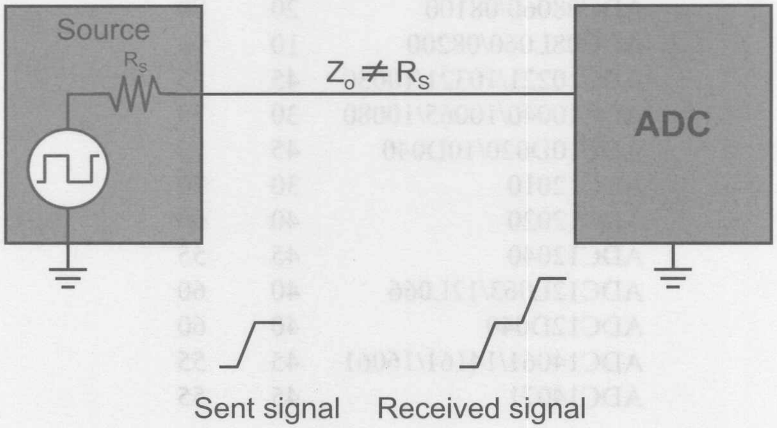
The ADC08100 family of ADCs from National Semiconductor will perform well over an extremely wide range of duty cycles.

High-Speed ADC Duty Cycle Range (Not All Products)

DEVICE	MIN.	MAX
ADC08060/08100	20	80
ADC08L060/08200	10	90
ADC10221/10321/10030	45	55
ADC10040/10065/10080	30	70
ADC10D020/10D040	45	55
ADC12010	30	70
ADC12020	40	60
ADC12040	45	55
ADC12L063/12L066	40	60
ADC12D040	40	60
ADC14061/14161/16061	45	55
ADC14071	45	55

This is a list of duty cycle ranges for some of National Semiconductor's high speed ADCs. Not all of them have extremely wide duty cycle tolerance, but they all have at least 45%/55% tolerances that ease the design task.

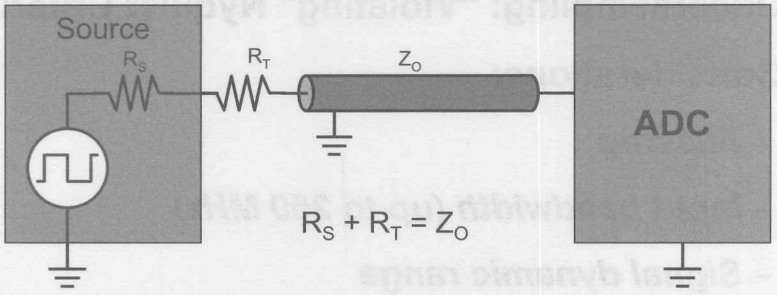
Signal Integrity Problem



All interconnecting lines are transmission lines. If the transmission line characteristic impedance (Z_O) is not matched to the signal source impedance or the signal receiver input impedance, there will be reflections on the line that cause distortion and even amplitude doubling of the signal. We say that the integrity of the signal is lost. This could cause any number of problems in a system.

In the case of the ADC clock line, this mismatch can result in noise, missing codes or erratic operation.

Maintaining Signal Integrity



$$R_S + R_T = Z_O$$

Treat the connection as a transmission line

Adding a terminating resistor such that its value plus the signal source impedance equals the characteristic impedance of the transmission line will usually ensure the integrity of the signal and prevent problems.

Undersampling Considerations

- **Undersampling: “Violating” Nyquist Criteria**
- **Considerations:**
  - *Aliasing*
  - *Input bandwidth (up to 250 MHz)*
  - *Signal dynamic range*

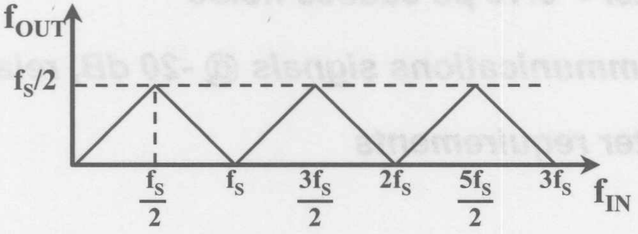
The Sampling Theorem says that, to preserve the frequency information in a signal, it must be sampled at a minimum of twice the highest frequency component in the signal. When the sample rate is not at least this high, all frequencies present will appear as some frequency lower than it originally was. This frequency conversion is called “aliasing”.

Some applications, such as communications, use aliasing to perform useful functions. For example, presenting an intermediate frequency of, say 250 MHz, to the input of an ADC that is sampled at a much lower rate can both demodulate the signal and digitize it at the same time.

These systems generally need to handle a wide dynamic range because the signal can be very weak at times and very strong at others.

Undersampling Considerations: Aliasing

- Sampling < 2 x highest input frequency
- $f_{OUT} \geq f_{IN} / 2$



$$f_{OUT} = |\, \mathrm{INT}(f_{IN} / f_S + 0.5) * f_S - f_{IN} \,|$$

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The highest frequency component that can appear at the output of an ADC is half the sample rate, or $f_S/2$, where f_S is the sample rate. The graph here is one of output frequency vs. input frequency. The output frequency can never exceed half the sample rate.

Undersampling Considerations: Input Bandwidth

- 250 MHz input undersampled to 12 Bits
  - *Jitter > 0.15 ps causes noise*
  - *Communications signals @ -20 dB, relaxing Jitter requirements*

It is not unusual to have communications systems with a 12-bit ADC operating at 60 to 70 MHZ with an input frequency in the range of 250 MHz. With an input frequency and resolution this high any jitter beyond 0.15 ps will degrade SNR performance of the ADC. While getting total jitter from all sources down to this level is an unattainable task, it is important to keep jitter to as low a level as we can.

Undersampling Considerations: Signal Dynamic Range

Min = Minimum signal level
Max = Maximum signal level

$$\text{Min resolution} = \text{LOG}_2\left(\frac{\text{Max}}{\text{Min}}\right)$$

or

$$\text{DR} = \text{dynamic range} = 20\text{LOG}_{10}\left(\frac{\text{Max}}{\text{Min}}\right)$$

$$\text{Min resolution} = \left(\frac{\text{DR (dB)}}{6.02\text{ (dB)}}\right)$$

The resolution requirements of the ADC is dictated by the weakest and strongest signals that must be accepted. Sometimes this means that an impossibly high resolution is required. To overcome this, designs use AGC (Automatic Gain Control).
The minimum resolution of the ADC then will depend upon the dynamic range requirements of the receiver and the gain variation provided by the ADC.

Undersampling Considerations: Signal Dynamic Range

Example: Maximum detectable signal: 2.0V
Minimum detectable signal: 100 uV

$$\text{Min Resolution} = \text{Log}_2 \left(\frac{2}{100\text{E-}6}\right) = 14.3 \text{ bits [need 16 bits]}$$

or

DR = 20Log(2/100E-6) /6.02 dB = 86 / 6.02 = 14.3 bits [need 16 bits]

Adding AGC so range is 500 uV to 1 V:

$$\text{Min Resolution} = \text{Log}_2 \left(\frac{1}{500\text{E-}6}\right) = 11 \text{ bits [use 12 bits]}$$

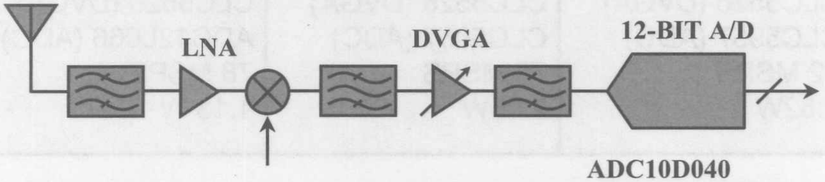
or

DR = 20Log(1/500E-6) /6.02 dB = 66 / 6.02 = 11 bits [use 12 bits]

This example shows the need for a 16 bit ADC, which may not be available at the desired sample rate. By adding an AGC loop we can reduce the resolution requirements to whatever is needed for other reasons.

High Speed ADCs Tackle Undersampling

- Up To 450MHz full power bandwidth (as opposed to analog input bandwidth)
- 60dB IMD performance
- 1.2 ps jitter
- Meets theoretical SNR vs. input level



ADC10D040
ADC10040/65/80
ADC12(D)040
ADC12L065
ADC12(D)L066
ADC12L080

Undersampling provides A/D conversion while demodulating the signal

Here we see a generalized block diagram of a communications receiver with some ADCs from National Semiconductor that might be used in these systems.
The theoretical SNR vs. Input is a 1 dB degradation in SNR performance for every 1 dB reduction in signal level.

DRCS / EDRCS / LDRCS

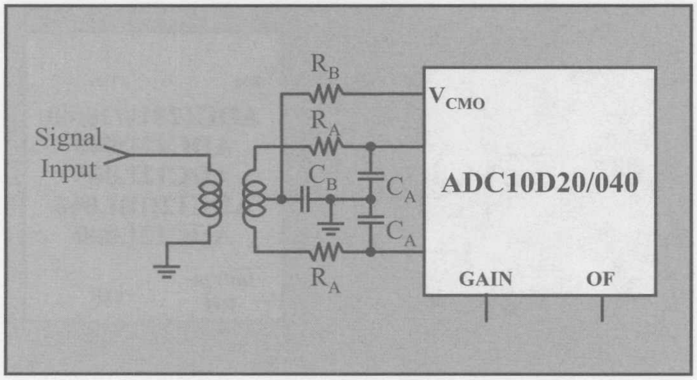
DRCS	EDRCS	LDRCS
Original	Extended Frequency	Low Power
CLC5902 (Tuner)	CLC5903 (Tuner)	CLC5903 (Tuner)
CLC5526 (DVGA)	CLC5526 (DVGA)	CLC5526 (DVGA)
CLC5957 (ADC)	CLC5957 (ADC)	ADC12L066 (ADC)
52 MSPS	78 MSPS	78 MSPS
2.52W	2.05W	1.13 W

Lowering power while extending operating frequency!

The DRCS (Diversity Receiver Chip Set), while an excellent solution, has been eclipsed by the EDRCS offering higher speed performance at a 20% power savings. The LDRCS provides even more power savings with the ADC12L066.

Finding A Common Mode Input Voltage - V_{CMO}

V_{CMO} - Common Mode Output



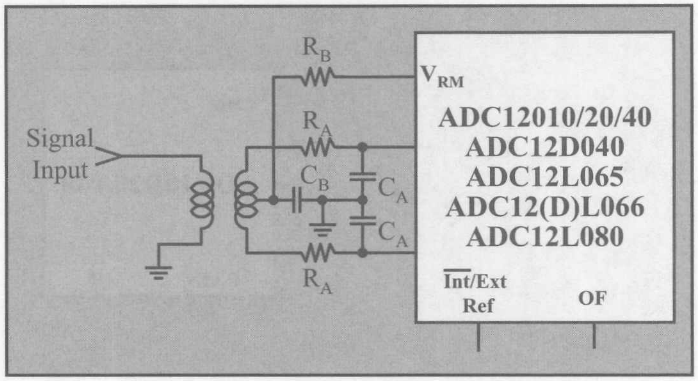
Some differential input ADCs have a fixed common mode input voltage on the die, while others operate well with a range of common mode voltages and allow the user to provide a common mode input voltage.

Examples of the latter devices include the ADC10D020 and ADC10D040. These products have a VCMO output that can be used as a common mode voltage. Furthermore, the VCMO output may be used as a voltage reference if the relatively large tempco can be tolerated.

RA and CA are used to counter the noise effects of the ADC input current pulses. A description of how to determine these values can be found in the data sheet of any of our high speed ADCs.

Finding A Common Mode Input Voltage - V_{RM}

- V_{RP}, V_{RM} and V_{RN} – Reference bypass pins



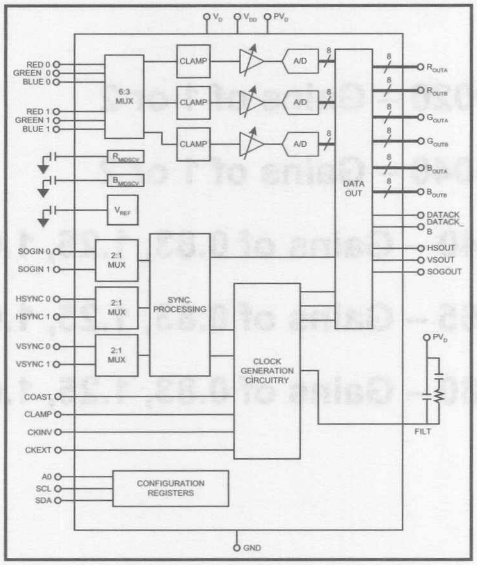
The devices indicated here have reference bypass pins that may not be loaded. However, the analog input currents of these products are just leakage currents, so the reference mid-point voltage, VRM, may be used as a common mode voltage source.

Not All ADCs Have Unity Gain

- ADC10D020 – Gains of 1 or 2
- ADC10D040 – Gains of 1 or 2
- ADC10040 – Gains of 0.83, 1.25, 1.67
- ADC10065 – Gains of 0.83, 1.25, 1.67
- ADC10080 – Gains of 0.83, 1.25, 1.67

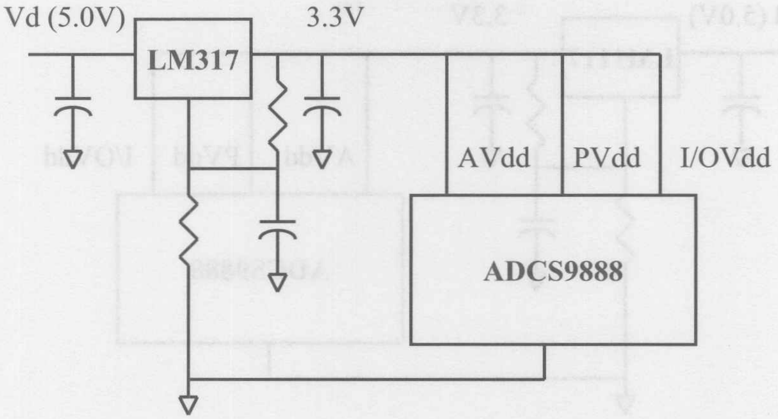
We generally assume that the gain of an ADC is unity. That is, we assume that a reference voltage of 1.0V means that the full-scale input voltage is 1.0Vp-p. However, this is not always the case. Sometimes the gain will even be user selectable, as in the examples indicated here.

Why is Power Important?



The ADCS9888 is a 3-channel video capture IC used in flat panel monitors, video projects, and other applications requiring the capture of high resolution video data. It has a 3-channel, 8-bit ADC section that operates at up to 205 MSPS. It also includes clock regeneration circuitry to create the high frequency pixel clock of 25 MHz to 205 MHz from the video synch. information. To perform these tasks, it has high speed analog and mixed signal circuitry, many high speed CMOS output drivers AND a noise sensitive PLL and on-chip VCO circuit. It is important to provide clean, noise-free power to the analog circuitry and the PLL/VCO. To do this, we need to make sure that noise from the 53 output drivers is not coupled into the analog supplies.

What's Wrong with This Picture?



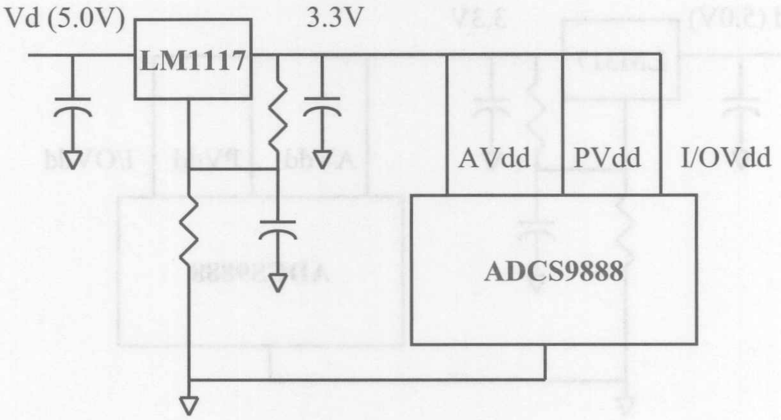
What is the easiest (cheapest?) way to provide power to this device. We can dig through our parts bin, and find a nice simple analog regulator to drop our +5V digital bus down to 3.3V for the circuitry in the ADCS9888. Is there anything wrong with this solution?

The biggest problem is the choice of regulator. The LM317 is a great device for many applications, but it is not a recommended device when dropping from 5V to 3.3V. Why?

The LM317 is a standard dropout voltage regulator, and generally needs at least two volts drop between Vin and Vout to regulate well. More is better. In this application, we have only a nominal 1.7V between Vin and Vout. This means that noise on the Vd bus can easily couple through the device and appear on the output. In IC specification terms the "line regulation" is terrible once we enter the dropout region.

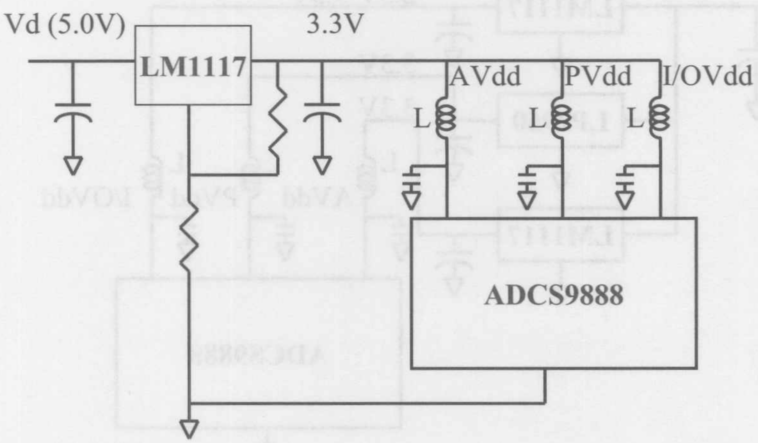
So what do we do?

Better Chance of Success



The quick-fix is to choose a different type of voltage regulator. The LM1117 is a quasi LDO (Low Dropout) regulator. This device will operate with dropout voltages in the range of 1.20V to 1.30 V depending on the load current and other factors. So now, the output 3.3V should have much less noise coupled in from the Vd bus. With adequate local high frequency decoupling between the Power and Ground pins on the ADCS9888, we have a much better chance of having a working system. But, there is still a potential for noise coupling between the different power buses on the chip.
What can we do to improve this?

Better Performance

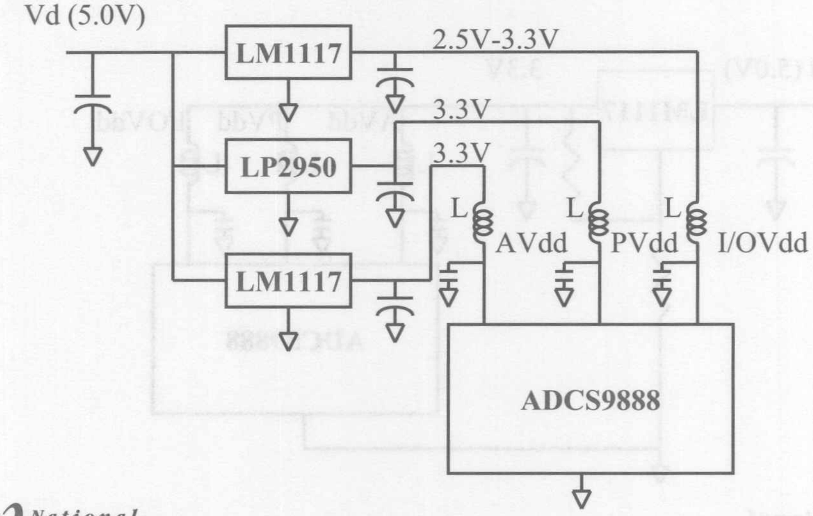


In addition to the local decoupling, we can add filter circuits on the individual power buses, and separate the three power buses into individual power planes. These planes can all be on the same printed circuit board layer, but will be isolated to reduce coupling. The filter networks will be located at the point where the common 3.3V Bus from the regulator is split into the three different buses for AVdd, PVdd and I/OVdd. Filter component values should be chosen to block the frequencies that could be generated by the noise sources, or that the analog circuitry is sensitive to.

This arrangement will provide improved performance in the ADC and also lower clock jitter in the PLL/VCO.

If we wanted to achieve even better performance, or be more assured of a achieving the performance we need on the first cut of the design, we could enhance this even further….

Best Performance



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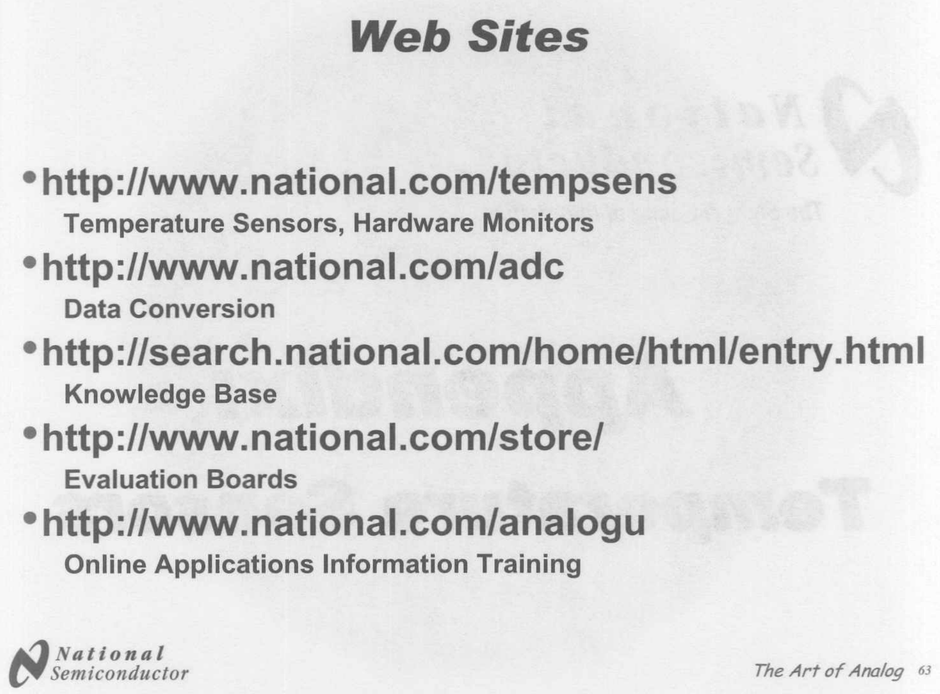
The ideal power solution would use individual voltage regulators to provide additional noise rejection between the different loads, and between the input voltage and the outputs. In addition, this solution allows the performance characteristics of the regulators to be optimized to the various loads. Higher current/low-cost-devices can be used for the loads that use more power, and are slightly less noise sensitive. A low noise regulator can be used for the sensitive PLL/VCO circuitry.



Web Sites

- **http://www.national.com/tempsens**
  Temperature Sensors, Hardware Monitors
- **http://www.national.com/adc**
  Data Conversion
- **http://search.national.com/home/html/entry.html**
  Knowledge Base
- **http://www.national.com/store/**
  Evaluation Boards
- **http://www.national.com/analogu**
  Online Applications Information Training

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These are just a few of the popular things that National Semiconductor has on its website. The first two here is for information regarding the indicated products. The "Knowledge Base" area features an intelligent search feature where you can enter your question in normal language. Access to other areas, such as a cross reference guide, can also be made from this page.

From our "store" you may purchase product evaluation boards.

Our Analog University offers online training in many areas.

Watch for expansion in all areas of our web site.

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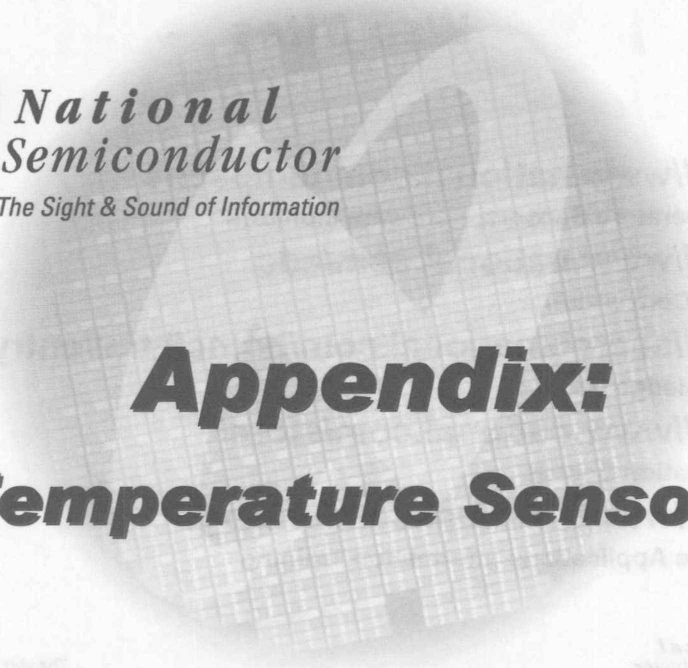
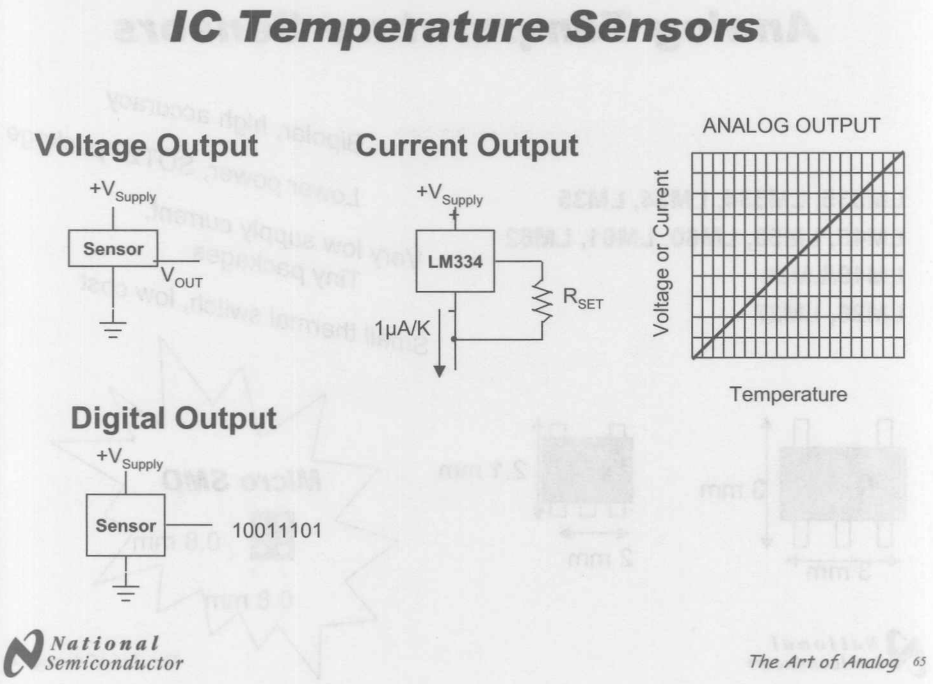
The Sight & Sound of Information



Appendix:

Temperature Sensors



IC Temperature Sensors

An IC temperature sensor measures temperature and outputs a signal which is proportional to that measured temperature. The output of the chip can be either analog or digital. An analog temperature sensor outputs a continuous signal (as opposed to a binary digital signal) in which the value of the signal is proportional to the temperature being measured. There are two types of analog outputs: voltage and current. A voltage output sensor has a voltage level at its output which varies up or down as the measured temperature varies. A current output sensor varies its current with the change in measured temperature.

A digital temperature sensor transmits a series of bits which comprise a digital word. The value of the digital word indicates the temperature that is being measured by the sensor. For example, as the measured temperature increases, the values of the digital word increases in proportion to the temperature. The length of the digital temperature word is dependent upon the resolution of the ADC in the temperature sensor. The digital temperature sensor family has a wide variety of products and features including, but not limited to, Remote Diode Temperature Sensors and System Health Monitors.

One of the most important specifications in a temperature sensor is its temperature measurement accuracy. That is, how close to the temperature being reported at the temperature sensor's output is to the actual temperature being measured. National Semiconductor is an industry innovator and leader in temperature sensor accuracy. Another important specification is operating temperature range. This is the range of temperatures that the sensor can measure and report. National Semiconductor temperature sensors operate over very wide temperature ranges with our temperature measurement extremes being –55°C to +300°C!

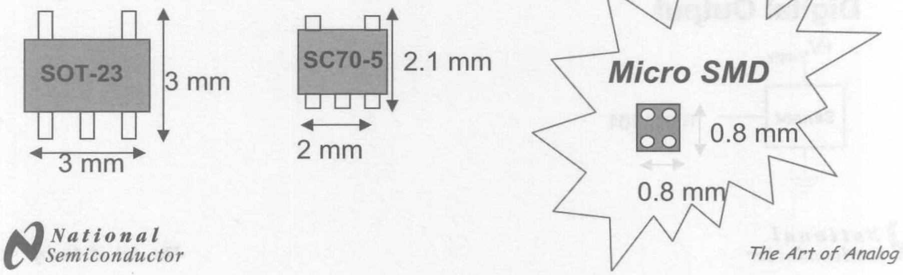
Analog Temperature Sensors

LM335, LM334, LM34, LM35 — Bipolar, high accuracy

LM45, LM50, LM60, LM61, LM62 — Lower power, SOT23 package

LM19/LM20 — Very low supply current, Tiny packages

LM26, LM27 — Small thermal switch, low cost

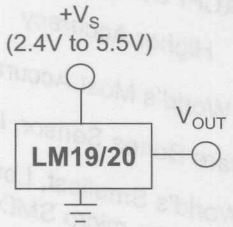


Analog temperature sensors are used everywhere, from cell phones and modems to vending machines and HVAC (heating, ventilation, and air conditioning) systems.

The performance of any electronic circuit varies as the temperature surrounding that circuit increases or decreases from some optimum temperature, usually room temperature. These performance variations often decrease the system's ability to function properly. With an IC temperature sensor incorporated into the system, the temperature can be measured, and corrective or compensating action can be applied by the system to maintain optimal performance.

The output of an analog temperature sensor is often connected to the input of an analog-to-digital converter or ADC. The ADC converts the analog voltage level to a digital word and that data is processed by the system's processor. In turn, the processor will increase, decrease, or maintain the speed of a fan to control the temperature. An advantage of analog temperature sensors is that their outputs can be directly connected to a temperature compensating circuit, bypassing the need for processor intervention.

LM19/LM20 Analog Temperature Sensor



- **LM20 replaces thermistor circuits**
- **Accurate: ±1.5°C and ±2.5°C at 30°C**
- **Very low supply current: less than 4.5 µA typical**
- **Small Packages: micro SMD, SC70, or TO-92.**

The LM20 is a low-cost, low-power analog temperature sensor that is used in a wide variety of applications. For example, it is often used to monitor the temperature of batteries, power amplifiers, and displays. It comes in 3 different grades with 2 different package options: SOT-23 and SC-70. The SC-70 package is about three fourths of the size of the SOT-23. Continuing on this path of smaller packages, we have also released the ultimate small package - the 4 lead micro SMD. This package is only slightly larger than the die itself, which is the size of a grain of sand.

The LM19 is similar to the LM20 except that it is available in a TO-92 package. The TO-92 package is useful in many industrial applications, such as control systems, HVAC, and smoke detectors. Both the LM20 and LM19 are great replacements for thermistors since they are more accurate over temperature. Also, the system designer does not have to worry about batch-to-batch testing of thermistors due to performance variations therein. System space and cost are reduced because the LM20 and the LM19 do not require external current limiting resistors or linearizing components such as an amplifier, as are often required in thermistor implementations of thermal management.

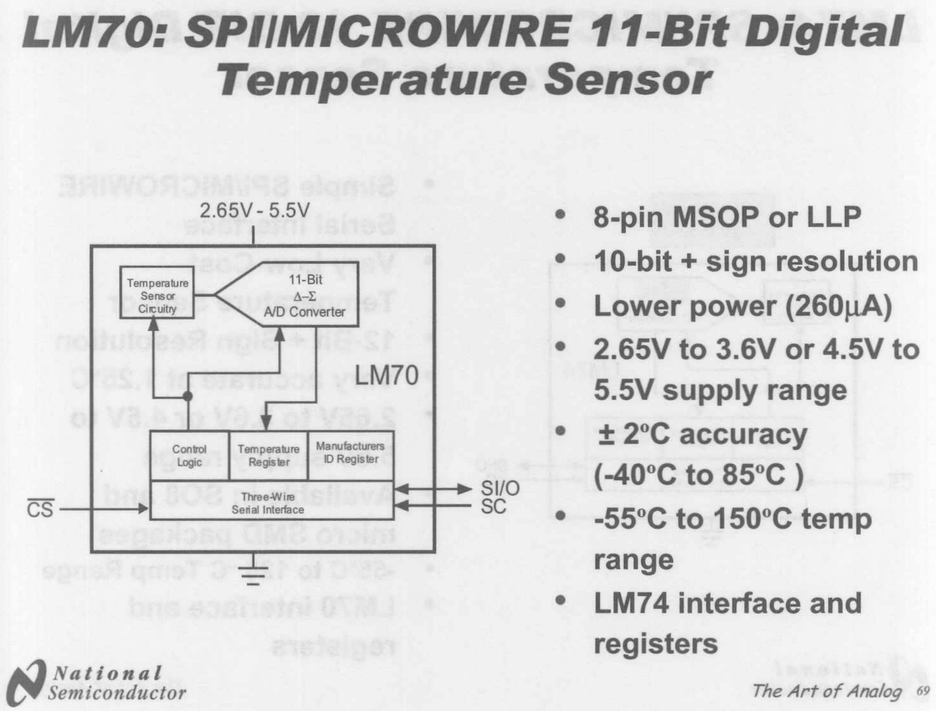
Digital Temperature Sensors

LM56: Dual Thermostat	Sensor & Comparator
LM75: 2-wire, 9b, 2.0°C	Industry Standard
LM77: 2-wire, 10b, 1.5°C	ACPI Compliance
LM76: 2-wire, 13b, 0.5°C & 1.0°C	Higher Accuracy
LM92: 2-wire, 13b, 0.33°C & 0.5°C	World's Most Accurate
LM70: 3-wire, 11b, 2.0°C	Bare Bones Sensor, LLP
LM74: 3-wire, 13b, 1.25°C	World's Smallest, Low Power, micro SMD

National Semiconductor offers a wide variety of Digital temperature sensors. Digital temperature sensors may interface directly to a system processor or microcontroller through a serial interface. Since the outputs are digital, no analog-to-digital converter is necessary to convert the temperature information to a digital format for processing by the system. National Semiconductor's wide range of digital temperature sensors incorporate many features while minimizing the development effort and chip count in system thermal management.

Applications include systems where an analog-to-digital converter is not available, cost-sensitive designs, designs requiring remote-diode sensing (like reading the temperature of a system processor), and applications requiring high accuracy.

National Semiconductor's digital temperature sensors use either of two serial interfaces, the three-wire SPI/MICROWIRE interface or the two-wire SMBus interface. From "simple" single temperature sensors to system hardware monitors, these products interface easily to the processor. Industry-leading small packaging saves valuable space on the system board.



LM70: SPI/MICROWIRE 11-Bit Digital Temperature Sensor

- **8-pin MSOP or LLP**
- **10-bit + sign resolution**
- **Lower power (260µA)**
- **2.65V to 3.6V or 4.5V to 5.5V supply range**
- **± 2°C accuracy (-40°C to 85°C)**
- **-55°C to 150°C temp range**
- **LM74 interface and registers**

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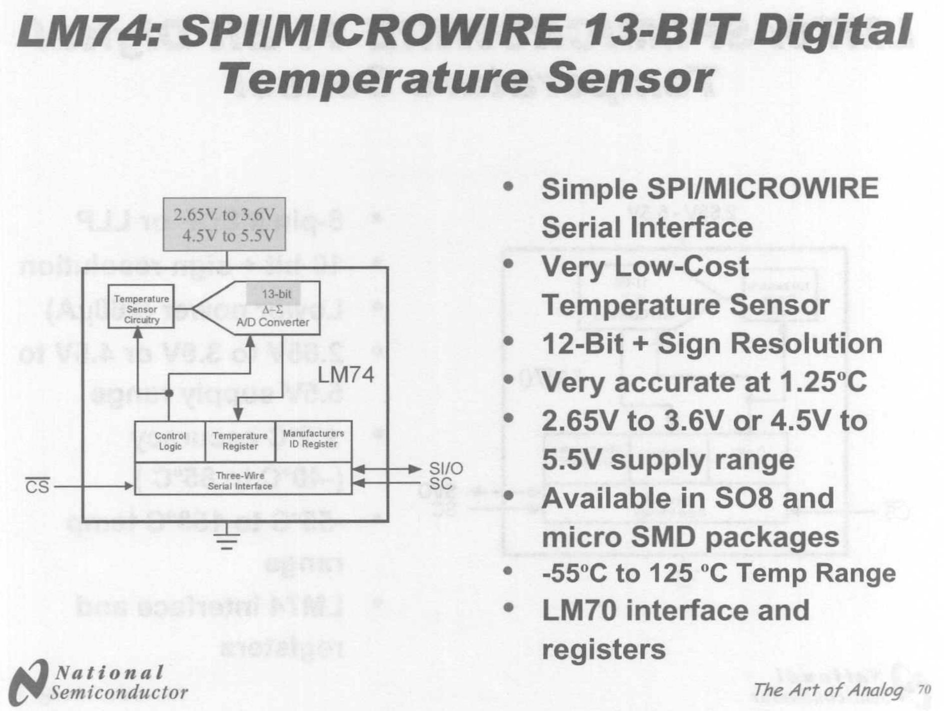
The LM70 digital temperature sensor is ideal for system thermal management in applications such as personal computers, disk drives, office electronics, and electronic test equipment. Its two-degree Celsius accuracy, wide power-supply range, and wide temperature range make it suitable for virtually any application. System processors and microcontrollers frequently have a built-in SPI/MICROWIRE interface and/or a general purpose I/O (GPIO) port. The processor can use either of these ports to communicate directly with, and read temperature from, the LM70 without the need for any other components.

The temperature is measured by an integrated band-gap temperature sensor, which feeds an analog voltage level (proportional to temperature) to an 11-bit delta-sigma ADC. The converter then feeds the data to the temperature register. The serial interface allows reading the temperature directly from the temperature register. The data is transmitted in two's complement format. The device will report the manufacturer's identification value to uniquely identify it as an LM70 when a read command is executed while the device is in shutdown

Power conservation is easily implemented when the processor commands the LM70 to go into shutdown mode. While in shutdown, the LM70 typically draws only 12µA of quiescent current. The shutdown mode is a significant advantage in the design of portable, battery-powered systems seeking extended battery life.



LM74: SPI/MICROWIRE 13-BIT Digital Temperature Sensor

- Simple SPI/MICROWIRE Serial Interface
- Very Low-Cost Temperature Sensor
- 12-Bit + Sign Resolution
- Very accurate at 1.25°C
- 2.65V to 3.6V or 4.5V to 5.5V supply range
- Available in SO8 and micro SMD packages
- -55°C to 125 °C Temp Range
- LM70 interface and registers

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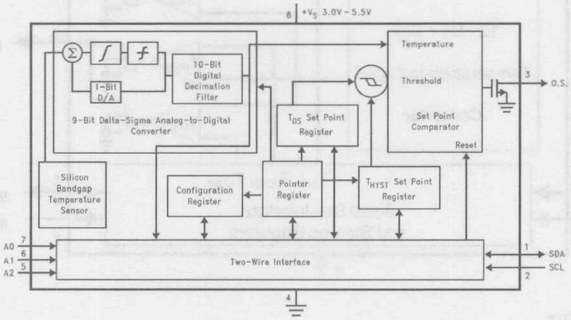
The Art of Analog 70

The LM74, like the LM70, finds applications across the full range of electronics systems where a processor or microcontroller needs to read the system temperature using a simple serial interface without additional components. The LM74 features an accuracy specification of 1.25 degrees Celsius. Its 13-bit resolution (twelve magnitude bits, plus a sign bit) allows the temperature to be read down to a fine 0.0625 degrees Celsius per bit, allowing very small temperature variations to be detected by the processor. The extremely small packaging, especially the micro SMD package at 1.6mm x 1.6mm, makes this temperature sensor particularly suited for systems where board space is at a premium. Communication with the LM74 uses the same format and register addresses as the LM70, so either can be used with just a few minimal software differences.

LM75B: Digital Temperature Sensor & Over-Temp Alarm

- ± 2°C accuracy (-25 °C to 100 °C)
- Low power (250μA)
- 3.0V to 5.5V supply range
- -55°C to 125 °C temp range
- Temperature sensor and thermostat functions
- Small packaging: SO8 and MSOP (3mm x 4.9mm)



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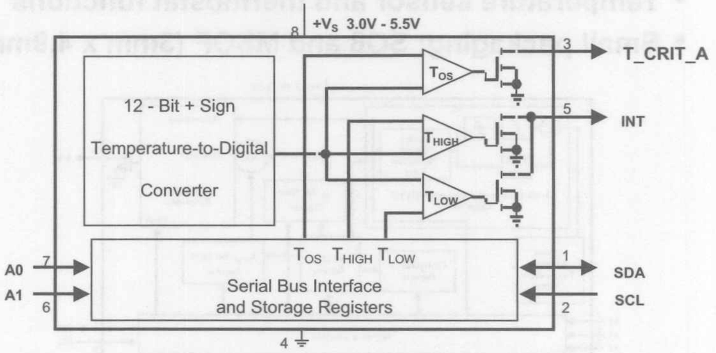
The LM75 is an extremely versatile temperature sensor which has become an industry standard for system thermal measurement in everything from PCs to vending machines. Its simple two-wire serial interface is compatible with the I^{2}C® protocol, which simplifies communication with the system processor. The over-temperature shutdown (O.S.) output tells the processor if the system's temperature has exceeded a user-programmed critical temperature. The over-temperature shutdown (O.S.) output can be polled by the processor or used as an interrupt. Programmable hysteresis is available to minimize system oscillation of the O.S. pin when near the programmed trip-point of the O.S. output.

A typical application would be where the processor is measuring system temperature through the serial interface during normal operation. If a mission-critical temperature is reached and some immediate action is required, say the cooling fan had failed, the O.S. pin will alert the system so that corrective action can be taken, like shutting down the system. The LM75 also has a shutdown mode. Shutdown mode reduces the quiescent current to only 4μA typical, which is very desirable in battery-powered systems.

The newer LM75B temperature sensor contains all the functionality of the older LM75C, plus three new additional features. First, the LM75B has an integrated low-pass filter on each of the serial communications lines, SDA and SCL. These filters greatly increase communications reliability in noisy environments. Second, a bus timeout feature has been implemented. If the SDA line is held low for longer than a specified time (325ms maximum), the LM75B will reset to the idle state and wait for a new start condition. In the event that the I^{2}C® serial bus in the system gets locked up, the sensor can escape the bus lock-up condition without the need for processor intervention. Third, the ESD susceptibility has been boosted from 1500V to 2500V (human body model). All of these features greatly enhance a system's reliability and it is advised that the LM75B, not the LM75C, be used for new designs.

LM92: World's Most Accurate Digital Temperature Sensor

- **Accuracy: ±0.33°C (max) at 30°C**
- **Patented error correction technique**
- **2.7V to 5.5V power supply voltage**
- **Shutdown mode reduces supply current to 4μA (typ)**
- **Manufacturers ID**



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The LM92 digital temperature sensor is the most accurate digital temperature on the market. Maximum errors of ±0.33ºC at 30ºC and ±1.0ºC from –10ºC to +85ºC are achieved. The LM92 is perfect for high accuracy applications such as temperature compensation of communication systems or temperature monitoring for process control.

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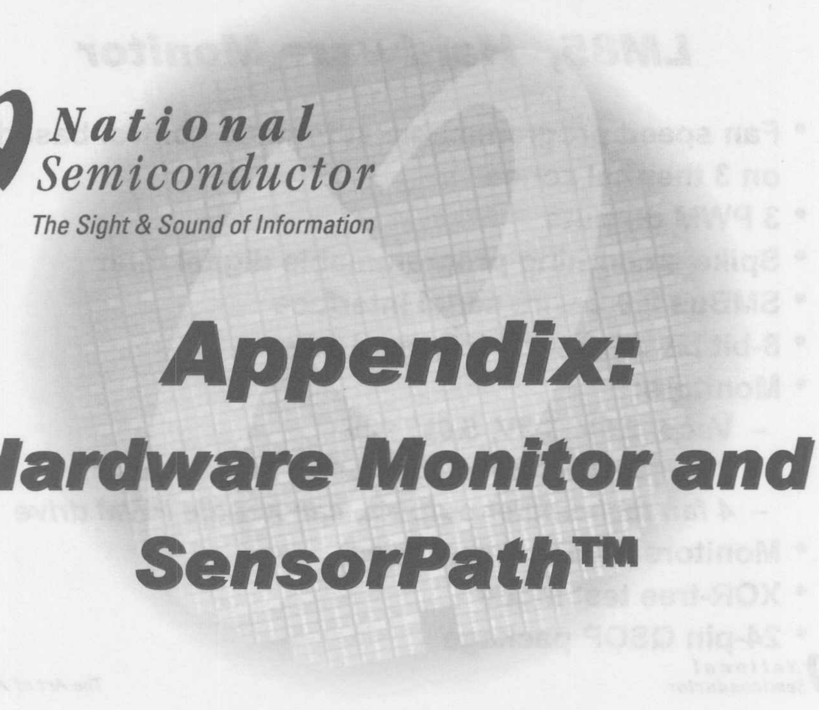
The Sight & Sound of Information



Appendix:

Hardware Monitor and SensorPath™

LM85, Hardware Monitor

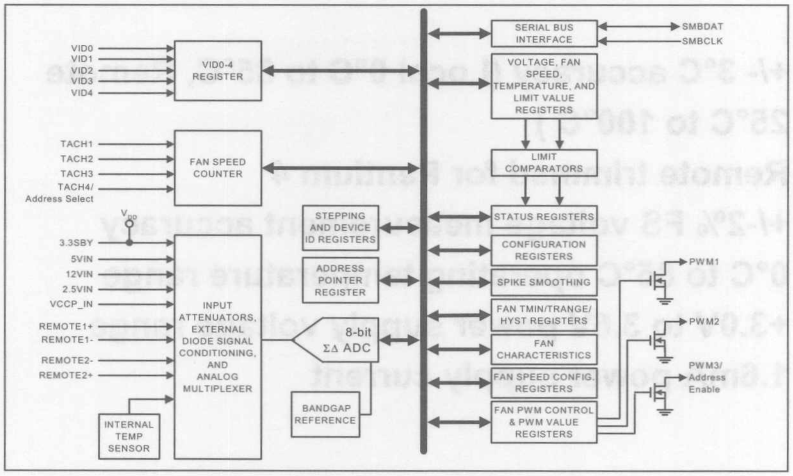
- **Fan speed programmable automatic control based on 3 thermal zones**
- **3 PWM outputs**
- **Spike smoothing programmable digital filter**
- **SMBus 2.0 2-wire serial interface**
- **8-bit ΣΔ ADC with 1°C resolution**
- **Monitors:**
  - ***Vccp, 2.5V, 3.3V, 5.0V, 12V***
  - ***2 remote thermal diodes and 1 local sensor***
  - ***4 fan tachometer outputs, can handle PWM drive***
- **Monitors 5 VID control lines**
- **XOR-tree test mode**
- **24-pin QSOP package**

The LM85 is a hardware monitor for the desktop PC market. The LM85 is not limited to this market; it may be used in any system where fan noise should be minimized. In our last seminar we discussed the LM87, which was targeted for the server market and is enjoying much success. The LM85 expands on the LM87 in that it includes programmable automatic fan control. It also includes an optional programmable digital filter for each temperature reading for fan speed control. An 8-bit Sigma-Delta ADC monitors, in a round-robin loop, 5 voltages, 2 remote diode temperatures as well as the die temperature of the LM85. Four tachometer inputs are simultaneously monitored and include circuitry for handling PWM drive.

LM85, Key Specifications

- +/- 3°C accuracy (Local 0°C to 85°C, Remote 25°C to 100°C)
- Remote trimmed for Pentium 4
- +/-2% FS voltage measurement accuracy
- 0°C to 85°C operating temperature range
- +3.0V to 3.6V power supply voltage range
- 1.6mA power supply current

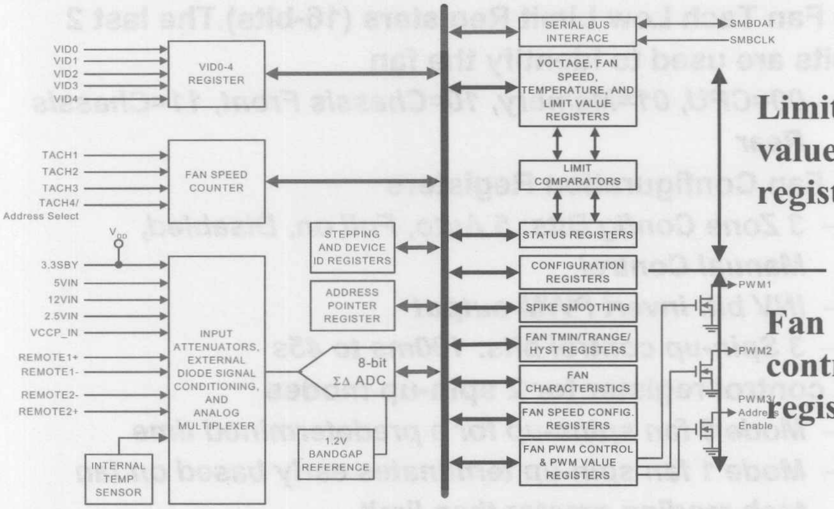
LM85: Block Diagram



NO interrupt output required with autonomous fan control!

The LM85 does not include EEPROM, therefore limits and fan settings need to be initialized by the BIOS after power up of the system.

LM85: Register Set



Limit and value registers

Fan control registers

Two status registers are provided to easily allow the Master controlling the LM85 to determine if everything is running properly. High and low limit registers for voltage and temperature measurements determine whether the appropriate status bits are set. Tachometer limits and fan speed control limits will also activate status bits.

Fan control registers are provided to allow the full autonomous operation of the PWM outputs that control fan speed. These registers will be discussed next.

LM85: Fan Control Registers

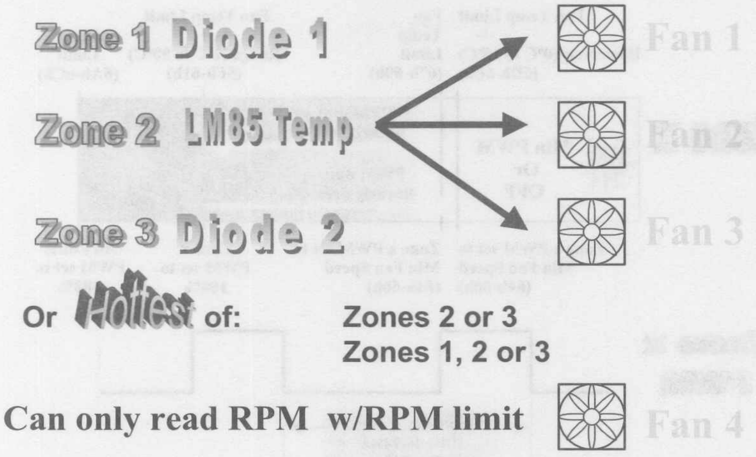
- **4 Fan Tach Low Limit Registers (16-bits).The last 2 bits are used to identify the fan**
  - ***00=CPU, 01=Memory, 10=Chassis Front, 11=Chassis Rear***
- **3 Fan Configuration Registers**
  - ***3 Zone Config Bits: 5 Auto, Full on, Disabled, Manual Control***
  - ***INV bit: invert PWM output***
  - ***3 Spin-up control bits: 100ms to 45s***
- **1 control register for 2 spin-up modes**
  - ***Mode 0 fan spins-up for a predetermined time***
  - ***Mode 1 fan spin-up terminates early based on fan tach reading greater than limit***

Let's start with the Fan Tachometer low limit registers. Not only do these registers determine what tachometer reading should set the status bit, but the last two bits of these registers determine which fan is being monitored. This value is programmed by the bios during initialization of the LM85. The 4 possible locations of a fan in a system include: CPU, Memory, Chassis Front or Chassis Rear.

Three Fan Configuration registers individually control the functionality of the three PWM outputs. Each register has 3 zone configuration bits that assign the temperature zone that controls the PWM output in Auto mode, set the PWM duty cycle to 100%, disable the PWM output or allow manual control, by the SMBus Master, of the PWM setting. The Auto modes are unique to this product.

Each register includes a INV or PWM output inversion bit that determines whether the PWM output is assigned a high level or a low level for 100% duty cycle. Note that if the system fails to initialize the LM85, the system may power on with the fan(s) at full speed. The three spin-up control bits determine the time interval the fan requires to overcome the turn on inertia. The LM85 has two spin up modes. Mode zero lets the PWM run at 100% duty cycle for the full programmed time interval. Mode one, on the other hand, aborts spin-up time interval once the tachometer reading exceeds the limit set in the Tach Low Limit Register for a particular fan.

LM85 Auto Mode Temperature Zone Assignments



Zone 1 Diode 1

Zone 2 LM85 Temp

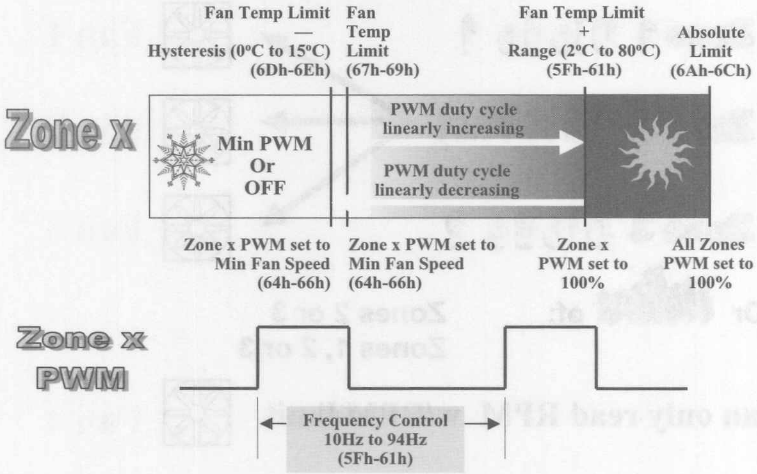
Zone 3 Diode 2

Or Hottest of: Zones 2 or 3
Zones 1, 2 or 3

Can only read RPM w/RPM limit

In the automatic mode each zone can be assigned to a fan. Any combination can be assigned. If need be all Fans 1 through 3 can be controlled by zone one. Two additional modes are provided. Any combination of fans can be controlled by the hottest of zones 2 or 3 in one mode or zones 1,2 or 3 in the other. Fan 4 in some systems may share the same zone as fan 3 therefore the same PWM control signal. You can only read the RPM of fan 4 and there is a Low Limit register and status bit associated with it.

LM85: Automatic Fan Control



Fan Temp Limit
—
Hysteresis (0°C to 15°C)
(6Dh-6Eh)

Fan
Temp
Limit
(67h-69h)

Fan Temp Limit
+
Range (2°C to 80°C)
(5Fh-61h)

Absolute
Limit
(6Ah-6Ch)

Zone x

Min PWM
Or
OFF

PWM duty cycle
linearly increasing

PWM duty cycle
linearly decreasing

Zone x PWM set to
Min Fan Speed
(64h-66h)

Zone x PWM set to
Min Fan Speed
(64h-66h)

Zone x
PWM set to
100%

All Zones
PWM set to
100%

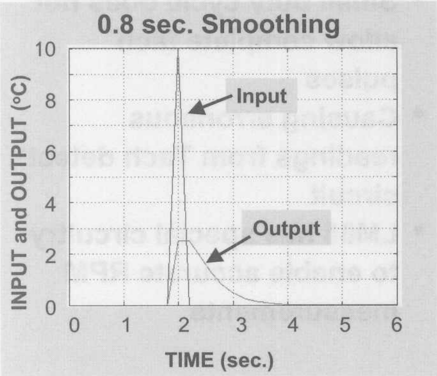
Zone x
PWM

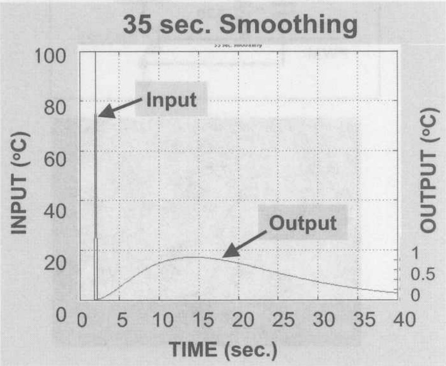
Frequency Control
10Hz to 94Hz
(5Fh-61h)

The LM85 fan control uses a linear algorithm. At low temperatures, the PWM output for a particular fan can be set in the off state or at a minimum value. Once the measured temperature of a particular zone exceeds the value set in the Fan Temp Limit register, the algorithm is enabled. The PWM duty cycle increases linearly until it reaches 100% when the temperature equals the Fan Temp Limit plus the value set in the Range register. The Range can have a value of 2oC to 80oC. There is an Absolute Limit for each zone, once any zone exceeds its limit all PWMs are set to 100%. If all zones are below their absolute maximum limit, then all PWM follow the Auto algorithm. As the temperature decreases, the PWM duty cycle will also linearly decrease. Once the temperature goes below the Fan Temp Limit minus the value set in the Hyst (Hysteresis) register, the fan will either turn off or remain at its minimum setting. There are 3 bits in register 62h that independently control whether each fan should be off or at min speed.
The PWM frequency for each output can be independently set between 10Hz to 94Hz.

Spike-Smoothing Filter

- Programmable smoothing only for fan speed control
- Smoothed temperature readings available
- Eight settings:
  35, 17.6, 11.8, 7.0, 4.4, 3.0, 1.6, 0.8 seconds





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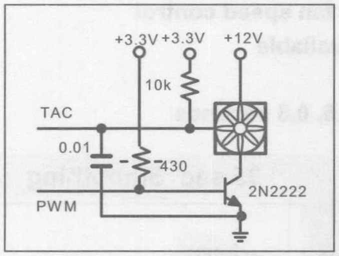
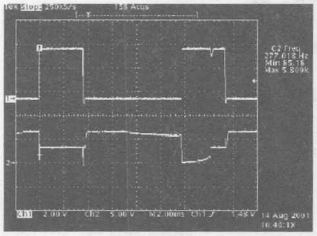
A smoothing filter with eight settings is available on the LM85 to be used to filter the temperature measurements that are used to determine the fan PWM setting. The digital output of this filter is not available to the user, only the un-smoothed number is.

Tachometer Input Signal





- Slow speed requires small duty cycle PWM
- Small duty cycle does not allow complete tach pulses
- Causing erroneous readings from Tach detect circuit
- LM85 has special circuitry to enable accurate RPM measurements

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When you control the fan speed with PWM low side drive (lowest cost solution), the GND of the fan floats, when the PWM signal is low, and the tachometer signal goes away. The actual voltage on the tach pin will go to the input level of the fan, 12V. This will cause the fan monitor to give erroneous results. The top trace of the scope photo shows the PWM drive signal and the bottom trace is the tachometer output. In this case the fan was spinning so slow that not even one complete tach pulse was captured when the 2N2222 turned on. The LM85 includes circuitry to accommodate this discontinuous fan tachometer signal. Smart tach modes require that the PWM1 output to be associated with the Tach1 input, PWM2 is associated with Tach2 and PWM3 is associated with Tach3 and Tach4 inputs in order to function properly.

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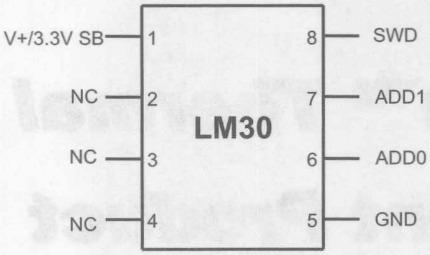
SensorPath™ Thermal Management Product Overview

This is a brief overview of the basics of SensorPath™. This section provides more details on the devices available from National Semiconductor that support SensorPath. More information on these devices as well as SensorPath can be found on the National Semiconductor web page www.national.com/appinfo/tempsensor.

LM30: Pinout and Features



- ±3°C from +0°C to +100°C
- 10-bit resolution, 0.25°C
- Internal ambient sensing
- Multiple address pins
- 8 Lead MSOP Package

Preliminary datasheet and samples available NOW!

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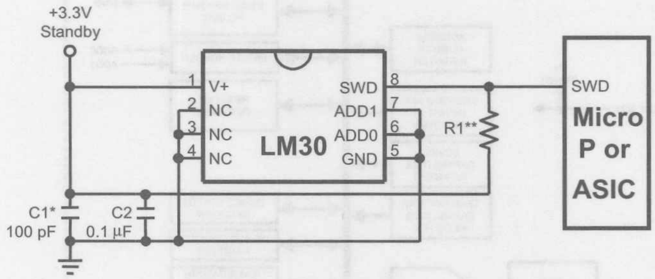
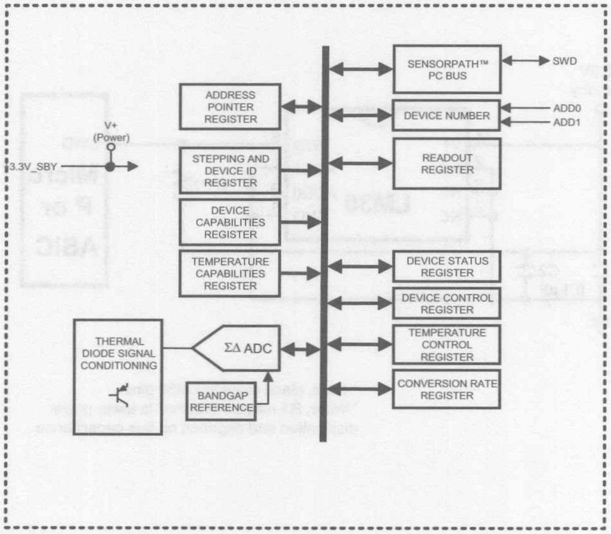
LM30: Typical Application Schematic



* Note, place close to LM30 pins

**Note, R1 may be required to lower power dissipation and depends on bus capacitance

LM30: Block Diagram



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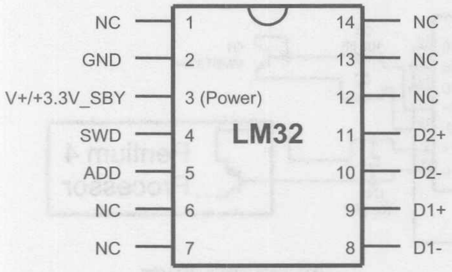
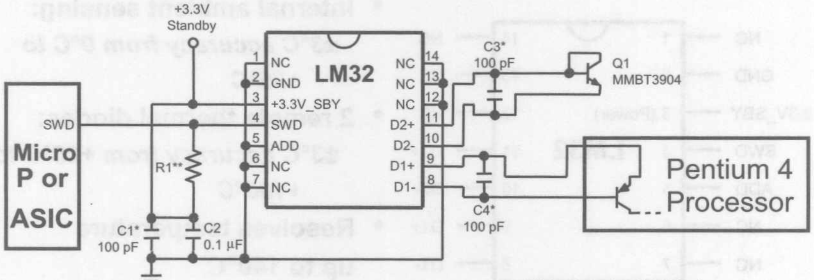
LM32: Pinout and Features



- Internal ambient sensing:
  - *±3°C accuracy from 0°C to +85°C*
- 2 remote thermal diodes:
  - *±3°C accuracy from +25°C to +100°C*
- Resolves temperature up to 140°C
- 10-bit resolution, 0.5°C
- Internal ambient sensing
- 14-Lead TSSOP Package

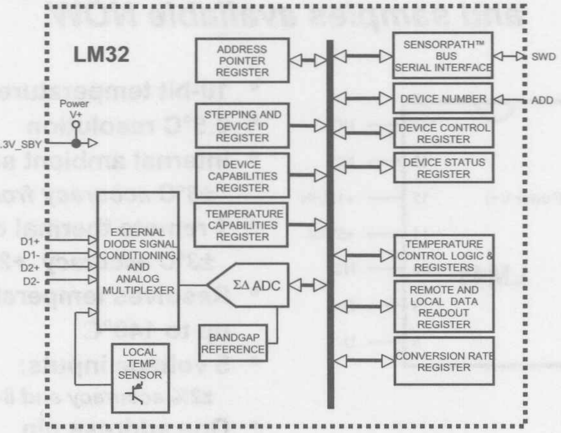
Preliminary datasheet
and samples available NOW.

LM32: Typical Application Schematic



* Note, place close to LM32 pins
**Note, R1 may be required to lower power dissipation and depends on bus capacitance

LM32: Block Diagram


LM32
Power
V+
+3.3V_SBY
ADDRESS POINTER REGISTER
STEPPING AND DEVICE ID REGISTER
DEVICE CAPABILITIES REGISTER
TEMPERATURE CAPABILITIES REGISTER
D1+
D1-
D2+
D2-
EXTERNAL DIODE SIGNAL CONDITIONING AND ANALOG MULTIPLEXER
ΣΔ ADC
BANDGAP REFERENCE
LOCAL TEMP SENSOR
SENSORPATH™ BUS SERIAL INTERFACE
SWD
DEVICE NUMBER
ADD
DEVICE CONTROL REGISTER
DEVICE STATUS REGISTER
TEMPERATURE CONTROL LOGIC & REGISTERS
REMOTE AND LOCAL DATA READOUT REGISTER
CONVERSION RATE REGISTER

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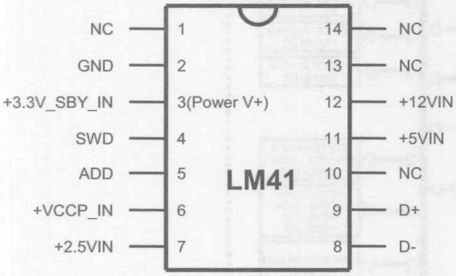
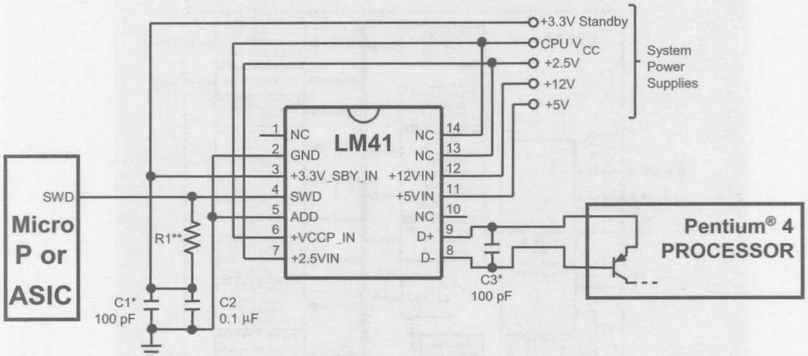
LM41: Pinout and Features

Preliminary datasheet and samples available NOW.



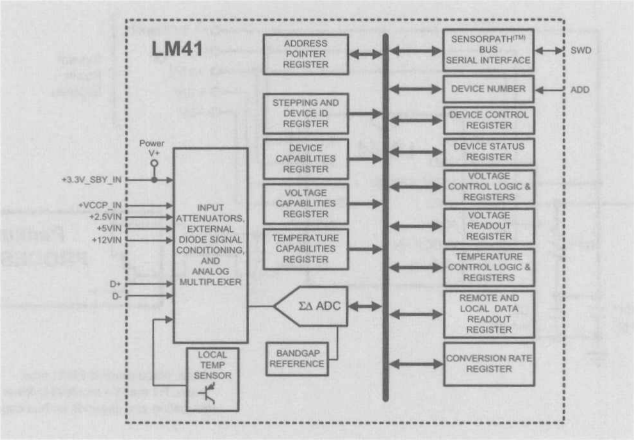
- **10-bit temperature**
- **0.5°C resolution**
- **Internal ambient sensing:**
  ±3°C accuracy from 0°C to +85°C
- **1 remote thermal diode:**
  ±3°C accuracy +25°C to +100°C
- **Resolves temperature up to 140°C**
- **5 voltage inputs:**
  ±2% accuracy and 8-bit resolution
- **One address pin**
- **14 Lead TSSOP package**

LM41: Typical Application Schematic

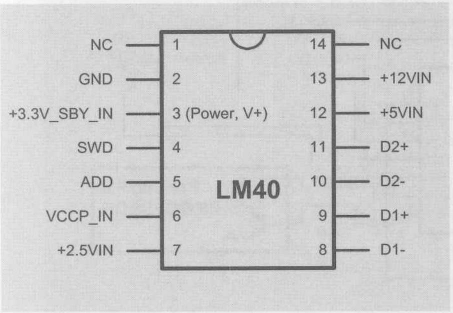


* Note, place close to LM41 pins.
**Note, R1 may be required to lower power dissipation and depends on bus capacitance.

LM41: Block Diagram


LM41
ADDRESS POINTER REGISTER
STEPPING AND DEVICE ID REGISTER
DEVICE CAPABILITIES REGISTER
VOLTAGE CAPABILITIES REGISTER
TEMPERATURE CAPABILITIES REGISTER
SENSORPATH(TM) BUS SERIAL INTERFACE
SWD
DEVICE NUMBER
ADD
DEVICE CONTROL REGISTER
DEVICE STATUS REGISTER
VOLTAGE CONTROL LOGIC & REGISTERS
VOLTAGE READOUT REGISTER
TEMPERATURE CONTROL LOGIC & REGISTERS
REMOTE AND LOCAL DATA READOUT REGISTER
CONVERSION RATE REGISTER
Power V+
+3.3V_SBY_IN
+VCCP_IN
+2.5VIN
+5VIN
+12VIN
D+
D-
INPUT ATTENUATORS, EXTERNAL DIODE SIGNAL CONDITIONING, AND ANALOG MULTIPLEXER
ΣΔ ADC
BANDGAP REFERENCE
LOCAL TEMP SENSOR

LM40: Pinout and Features



- **10-bit temperature**
- **0.5°C resolution**
- **Resolves temperature up to 140°C**
- **Internal ambient sensing:**
  - ***±3°C accuracy from 0°C to +85°C***
- **2 remote thermal diodes:**
  - ***±3°C accuracy +25°C to +100°C***
- **5 voltage inputs:**
  - ***±2% accuracy***
  - ***8-bit resolution***
- **One address pin**
- **14 Lead TSSOP Package**

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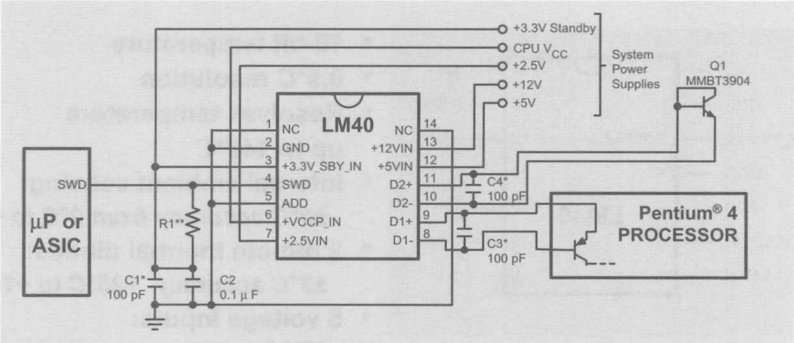
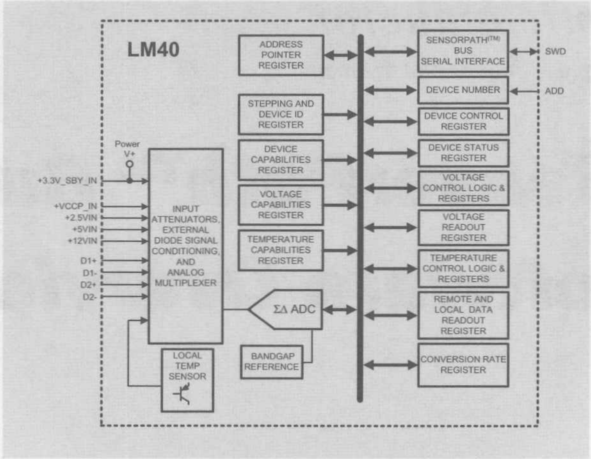
LM40: Typical Application Schematic



* Note, place close to LM40 pins.
**Note, R1 may be required to lower power dissipation and depends on bus capacitance.

LM40: Block Diagram


LM40
Power
V+
+3.3V_SBY_IN
+VCCP_IN
+2.5VIN
+5VIN
+12VIN
D1+
D1-
D2+
D2-
INPUT ATTENUATORS, EXTERNAL DIODE SIGNAL CONDITIONING, AND ANALOG MULTIPLEXER
LOCAL TEMP SENSOR
BANDGAP REFERENCE
ΣΔ ADC
ADDRESS POINTER REGISTER
STEPPING AND DEVICE ID REGISTER
DEVICE CAPABILITIES REGISTER
VOLTAGE CAPABILITIES REGISTER
TEMPERATURE CAPABILITIES REGISTER
SENSORPATH(TM) BUS SERIAL INTERFACE
SWD
DEVICE NUMBER
ADD
DEVICE CONTROL REGISTER
DEVICE STATUS REGISTER
VOLTAGE CONTROL LOGIC & REGISTERS
VOLTAGE READOUT REGISTER
TEMPERATURE CONTROL LOGIC & REGISTERS
REMOTE AND LOCAL DATA READOUT REGISTER
CONVERSION RATE REGISTER

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SensorPath™ Bus Software Overview

This overview covers the basics of the firmware implementation of the SensorPath™ protocol for the master. We will start at the bit level and work our way up to the write/read transaction.

Bit Output Routine

- Begin Loop
- Wait for SensorPath™ inactive
- Start output timer and drive SensorPath low
- When output timer done, release bus
- Wait for inactive bus and read pulse timer
- If attention bit received, restart loop
- If valid bit received, return bit //success
- Else return FAILURE
- End Loop

The SensorPath™ master bit output consists of:
Wait for the bus to be inactive (high) for the minimum time
Set a timer to the appropriate time for the bit
Start the timer and then drive the bus low
When timer expires, release the bus
Wait for the inactive bus and read the timing of the output pulse (from interrupt routine)
If an attention bit is received, resend output bit from the start of the loop
If a valid bit was received, return the bit type
Else return an error

Bit Input Routine

- Use bit output routine to output bit 0
- If the bit is read as 0 or 1 , return bit
- Else return FAILURE

The SensorPath™ master bit input consists of:
Output a bit 0
Read the same bit which is 0 if the device leaves the bus high, or is 1 if the device drives the bus low for the bit 1 time.

Write Transaction Routine

- **Begin Retry Loop**
- **//Note: if any bit error occurs, restart loop**
- **Output start, device, address, write bits**
- **Output data, parity bits**
- **Input ack bit**
- **If bit is 1, return SUCCESS**
- **If retry count < max, restart loop**
- **Else return FAILURE**
- **End Retry Loop**

The SensorPath™ master write transaction consists of:
Write a start bit, 3 device bits, 6 address bits, a write bit, 8 or 16 data bits, and a parity bit.
Read an ack/nack bit back from the device.
When a bit or nack error occurs, the transaction can be retried x times.

Read Transaction Routine

- Begin retry loop
- //Note: if any bit error occurs, restart loop
- Output start, device, address, read bits
- Input data, parity bits
- If parity is correct, output ack bit
- If ack bit is 1, return SUCCESS
- If retry count < max, restart loop
- Else return FAILURE
- End retry loop

The SensorPath™ master read transaction consists of:
Write a start bit, 3 device bits, 6 address bits and a read bit.
Read 8 or 16 data bits, and a parity bit.
Write an ack if the parity is valid
When a bit or parity error occurs, the transaction can be retried x times.

Idle loop for Attention

- If attention flag set
- Loop through all devices
- Read status register for device
- For all enabled Status Function bits,
- Read the data readout register
- End Loop
- End If

The attention bit is processed during idle time. If an attention has occurred, the status register for each device is checked. If the Status Function bit is set, the appropriate data readout register is read.

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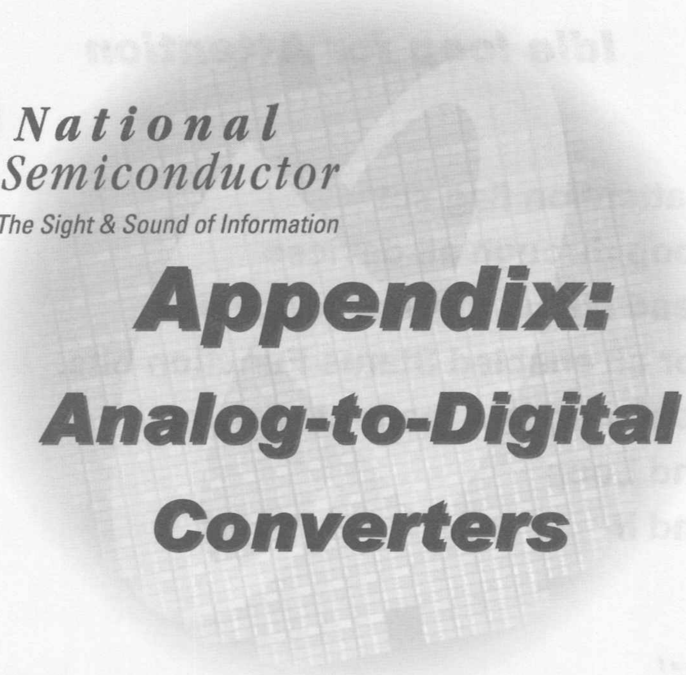
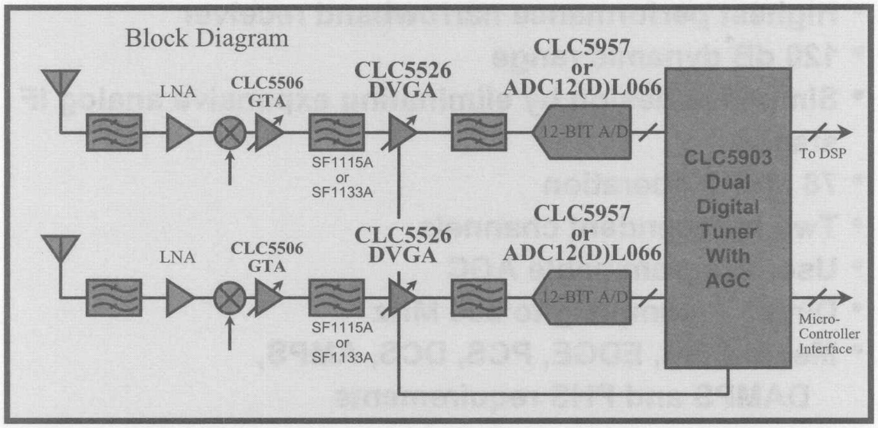


Appendix: Analog-to-Digital Converters

Diversity Receiver Chip Set



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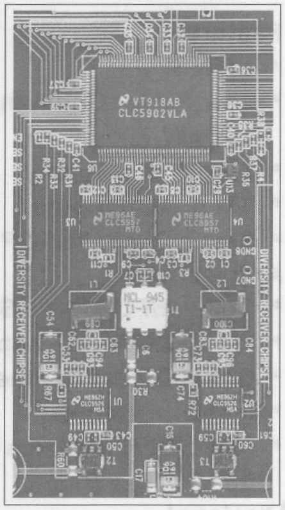
Our diversity receiver chip set provides two independent receiver channels. It was originally designed using the CLC5957 as the A/D converter, but the ADC12L066 provides a lower power solution. Further, the ADC12DL066 provides two ADCs in a single package, reducing board space and further reducing power consumption.

Diversity Receiver

- Highest performance narrowband receiver
- 120 dB dynamic range
- Simplifies design by eliminating expensive analog IF stages
- 78 MSPS operation
- Two independent channels
- User Programmable AGC
- Direct IF-sampling to 300 MHz
- Meets GSM, EDGE, PCS, DCS, AMPS, DAMPS and PHS requirements

Our Diversity Receiver chip set offers the highest level of performance currently available. The 120 dB dynamic range is provided by the 12-bit ADC and a PGA (Programmable Gain Amplifier).

CLC5526, CLC5957 / ADC12L066 / ADC12DL066, and CLC5903 Enhanced Diversity Receiver Chipset



Features

- 78MSPS Operation
- Two Independent Down Converter Channels
- Independent Channel Filters
- Wide Dynamic Range: >120dB at 150MHz
- Programmable AGC
- Meets GSM/EDGE, PCS, AMPS, DAMPS, and PHS Cellular Specifications

Applications

- Cellular Basestations
- Satellite Receivers
- Paging Basestations
- Wireless Local Loop Receivers
- Digital Communications

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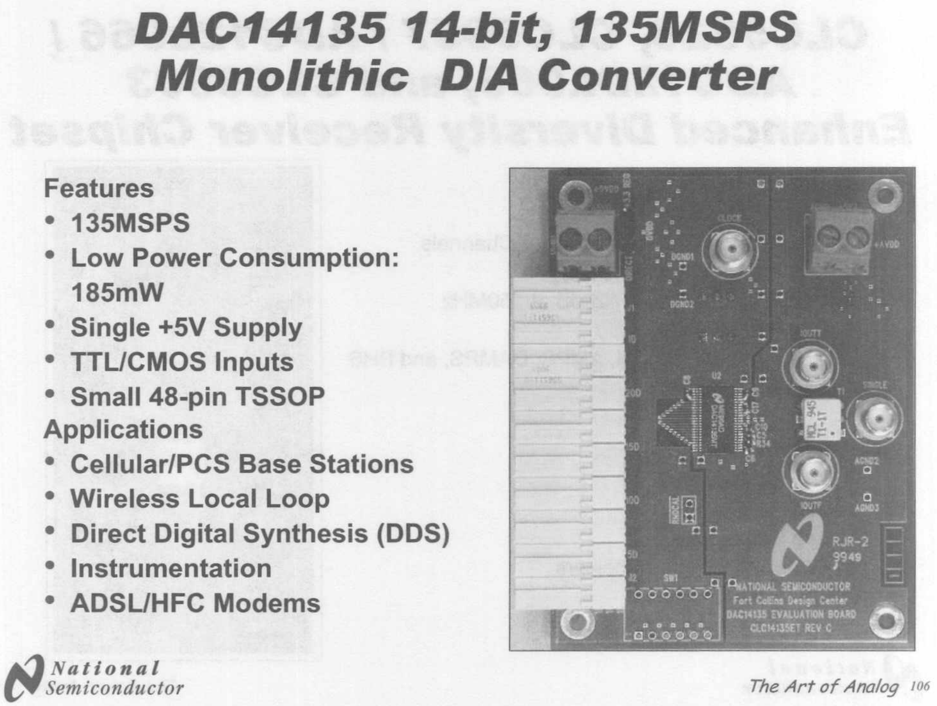
The Art of Analog 105

The ADC12L066 replaces the CLC5957 for lower power consumption. A space saving can be accomplished by using the ADC12DL066 in place of two ADC12L066s.



DAC14135 14-bit, 135MSPS Monolithic D/A Converter

Features

- 135MSPS
- Low Power Consumption: 185mW
- Single +5V Supply
- TTL/CMOS Inputs
- Small 48-pin TSSOP

Applications

- Cellular/PCS Base Stations
- Wireless Local Loop
- Direct Digital Synthesis (DDS)
- Instrumentation
- ADSL/HFC Modems

National Semiconductor

The Art of Analog 106

The DAC14135 is our only high speed DAC offering at this time. It offers excellent performance at a very reasonable price. The price is low enough to compete with 10-bit high speed DACs.

National's Infrastructure Products

- Analog to digital converters
  - *CLC5957 12-bit, 70 MSPS*
  - *ADC12L063, 12-bit, 62 MSPS*
  - *ADC12L066, 12-bit, 66 MSPS*
  - *ADC12DL066, Dual 12-bit 66 MSPS*
- Digitally programmable IF amplifiers
  - *CLC5526 350 MHz, 6 dB steps*
- Digital downconverters
  - *CLC5903 Dual 78 MSPS, >120 dB Dynamic Range*
- Digital-to-analog converter
  - *DAC14135 14-bit, 135 MSPS*

National offers a complete solution for wireless infrastructure.

ADC Product Summary
High Speed, 8-Bits

DEVICE	RES	SPEED MSPS	PWR mW	FPBW MHz	SNR dB	THD dB	SINAD dB	ENOB dB	@ FREQ dB
ADC1173	8	15	36	120	48.7	-54	47.7	7.6	3.6
ADC1175	8	20	60	120	42	-52	45	7.2	9.9
ADC08351	8	42	40	120	45	-51	45	7.2	4.4
ADC1175-50	8	50	125	120	44	-51	43	6.8	24.9
ADC08060	8	60	1.3/MSPS	200	47	-57	47	7.5	25
ADC08L060	8	60	1.05/MSPS	270	47.2	-53.3	46.1	7.4	29
ADC08100	8	100	1.3/MSPS	200	46.5	-60	46	7.3	41
ADC08200	8	200	1.05/MSPS	500	46	-60	46	7.3	50

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This and the following slides are mini selection guides. The last column is the frequency at which the dynamic performance characteristics are specified.

Of course, we are constantly introducing new products, so contact your local sales engineer for updates.

ADC Product Summary
High Speed – 10-Bits

		SPEED	PWR	FPBW	SNR	THD	SINAD	ENOB	@ FREQ
DEVICE	**RES**	**MSPS**	**mW**	**MHz**	**dB**	**dB**	**dB**	**dB**	**dB**
ADC10221	10	15	98	150	60	-70	59	9.5	4.4
ADC10321	10	20	98	150	60	-70	59	9.5	4.4
ADC10D020	10x2	20	150	140	59	-73	59	9.5	19.5
ADC10030	10	27	125	150	59	-66	58	9.4	13.5
ADC10D040	10x2	40	267	140	60	-69	59	9.5	10.4
ADC10040	10	40	55.5	400	59.6	-77	59.4	9.6	19
ADC10065	10	65	68.6	400	59.3	-72	59	9.5	32
ADC10080	10	80	78.6	400	59.2	64.7	59	9.5	39

ADC Product Summary
High Speed – 12-Bits

DEVICE	RES	SPEED MSPS	FPBW MHz	PWR mW	SNR dB	THD dB	SINAD dB	ENOB dB	@ FREQ dB
ADC12081	12	5	100	105	68	-79	67.6	10.9	2.5
ADC12181	12	10	100	235	65	-74	64.5	10.4	5
ADC12191	12	10	100	235	63	-72	62	10	5
ADC12010	12	10	100	160	70	-83	69	11.2	10.1
ADC12281	12	20	100	443	65.5	-76	65	10.5	4.4
ADC12020	12	20	100	185	70	-83	69	11.2	10.1
ADC12040	12	40	100	340	69.5	-80	69	11.2	10
ADC12D040	12x2	40	100	600	68	-78	68	10.9	10
ADC12L063	12	62	170	354	66	-74	65	10.3	10
ADC12L065 *	12	65	300	165	65	-70	64	10.3	16.5
ADC12L066	12	66	450	357	65	-71	64	10.3	25
*ADC12DL066**	12x2	66	450	650	64	-71	63	10.2	33
ADC12L080 *	12	80	450	350	63	-70	63	10.2	50

** Preliminary at time of Preparation*

ADC Product Summary
High Speed – 14- and 16-Bits

DEVICE	RES	SPEED MSPS	PWR mW	FPBW MHz	SNR dB	THD dB	SINAD dB	ENOB dB	@ FREQ dB
ADC14061	14	2.5	390	8	80	-88	79	12.8	500k
ADC14161	14	2.5	390	8	80	-88	79	12.8	500k
ADC14071	14	7.5	380	25	77	-79	74	12.0	3.5M
ADC16061	16	2.7	390	45	80	-88	79	12.8	500k

ADC Product Summary
Newer Industrial

DEVICE	RES	SPEED MSPS	FPBW MHz	SNR dB	THD dB	SINAD dB	ENOB dB	@ FREQ dB
ADCS7476	12	1.0	8	72.5	-80	72	11.6	100k
ADCS7477	10	1.0	8	62	-77	61.7	10.0	100k
ADCS7478	8	1.0	8	49.7	-77	49.7	8.0	100k
ADC74H89	12	0.5	8	72.8	-86	72.6	11.8	40k
ADCS7887 *	12	0.125	3	72	-82	71.6	11.6	10k
ADC7888 *	12x2	0.125	3	72	-82	71.6	11.6	10k

* Preliminary at time of Preparation

ADC Glossary of Terms

Absolute Maximum Ratings – Voltages and currents beyond which a device may not be stressed without danger of damaging or destroying the device. The device is NOT guaranteed to work when stressed at or near its absolute maximum ratings..

A/D – See ADC.

A/D Converter – See ADC.

A.C. Termination – Transmission line termination technique where a series RC is used at the receiving end of a transmission line.

A.C. Termination – Transmission line termination technique where a series RC is used at the receiving end of a transmission line.

ADC – Analog-to-Digital Converter. A device or circuit used to convert analog information to digital words.

Aliasing – Conversion of an input frequency to another frequency as a result of the conversion process. The output frequency of an ADC can never exceed ½ the sampling frequency of the ADC without this aliasing. When the input frequency does exceed ½ the sampling frequency, the output frequency becomes the absolute value of $[\mathrm{INT}(f_{IN}/f_S + 0.5) * f_S - f_{IN}]$.

Characteristic Impedance - The impedance a transmission line such that, when driven by a circuit with that output impedance, the line appears to be of infinite length such that it will have no standing waves, no reflections from the end and a constant ratio of voltage to current at a given frequency at every point on the line.

DAC – Digital-to-Analog Converter. A device or circuit used to convert digital words into analog voltages or currents.

Director – The shorter elements of a "Yagi" antenna that directs energy toward the driven element.

DLE – Differential Linearity Error. Same as DNL.

DNL – Differential Non-Linearity. The measure of the maximum deviation from the ideal step size of 1.00 LSB.

ENOB – Effective Number Of Bits. A specification that helps to quantify dynamic performance. ENOB says that the converter performs as if it were a theoretically perfect converter with a resolution of ENOB. That is, an ENOB of 7.4 says that the converter performs, as far as SINAD is concerned, as if it were a perfectly ideal ADC with a resolution of 7.4 bits (assuming you could have fractional bits). The idea behind ENOB comes from the fact that the absolutely perfect ADC has an SNR that comes only from quantization noise and has absolutely no distortion. When this is the case, SINAD is then equal to SNR. Since SNR of the absolutely perfect ADC is SNR = 6.02 * n +1.76, where "n" is the number of ADC output data bits, SINAD = SNR for a perfect converter, so SINAD = 6.02 * n + 1.76 and n = (SINAD – 1.76) / 6.02 and we say that ENOB = (SINAD – 1.76) / 6.02 .

FFT – Fast Fourier Transform. The FFT is a mathematical operation that converts signals between the time and frequency domains. We generally call the frequency domain (amplitude vs. frequency) plot an FFT.

EMI/RFI – Electromagnetic Interference/Radio Frequency Interference. This is the radiation of EM (electromagnetic) energy that may interfere with other circuits and systems.

FR-4 – A glass epoxy printed circuit board material of woven glass cloth construction laminate with an epoxy resin binder.

Full-Scale Input Swing – The difference between the maximum and minimum input voltages that will produce a valid ADC output without going over- or under-range.

Gain Error - The error in the slope of the ADC transfer characteristic. It is the difference in the actual and ideal full scale input range values.

IMD – Intermodulation Distortion. This is the creation of new spectral components that result from two or more input frequencies modulating each other when the circuit is nonlinear.

ILE – Integral Linearity Error.This is the same as INL.

INL – Integral Non-Linearity. The maximum departure of the ADC transfer curve from the ideal transfer curve. INL is a measure of how straight is the transfer function curve. There are two popular methods of measuring INL: End Point and Best Fit. The End-Point method is the most conservative, while the Best Fit method gives lower (better-looking) values. National uses the End Point method.

ADC Glossary of Terms (2)

Input Dynamic Range – For an ADC, the range of voltages that can be applied to the input without going under or over range.

Input Offset – The difference between the input value of 1.0 LSB and the input voltage that causes the ADC output code to transition from zero to the first code. Input Offset Error – The difference between the ideal input value of 0.5 LSB and the input voltage that causes the ADC output code to transition from zero to the first code.

Jitter – The variation in the timing of a signal's rising or falling edge. It can be specified as cycle-to-cycle or long term.

Loop Area – The area between the conductors of outgoing and return currents.

LSB – Least Significant Bit. The bit that has the least weight.

Missing Codes – Those ADC codes that never appear at the ADC output. These codes can not be obtained with any input value.

Nyquist Rate –The minimum sampling rate (or frequency) needed to prevent frequency aliasing.

Nyquist Frequency –The maximum input frequency beyond which frequency aliasing results.

Offset Error – This is the same as Input Offset Error.

PC Board – Printed Circuit Board.

PCB – Printed Circuit Board.

Proximity Effect – The phenomenon whereby outgoing and return currents want to flow close to each other.

PSRR – Power Supply Rejection Ratio. A measure of how well a circuit rejects a signal on its power supply. There are two ways to specify PSRR, the most common of which is to specify the change in one parameter when the d.c. value of the power supply is changed. That is, one value of d.c. voltage is applied to the supply pins and the selected parameter (e.g. offset error) is measured. Then another d.c. voltage is applied to the supply pins and the same parameter is again measured. The extent to which the selected parameter does not change when the supply voltage is changed is the d.c. PSRR. This tells us nothing about how well an a.c. signal, such as noise, on the supply line will be rejected by the device.

The other method is the specify how an a.c. signal on the power supply will affect the output of the device. National specifies both methods for most of our ADCs. This provides the all-important a.c. PSRR, but also provides d.c. PSRR that may be compared with competition. Note, however, that the two readings have no relationship to each other.

Quantization – The process of dividing a range of analog voltages or currents into smaller "quanta" (smaller range of voltages or currents) such that each quanta is represented by a single digital code.

Quantization Error – The error introduced as a result of the quantization process. The amount of this error is a function of the resolution of the quantizer. By definition, the quantization error of an ADC is ½ LSB.

Quantization Noise – The noise at the ADC output that is caused by the quantization process. It is defined as 20 * log ($2^{(n-1)}$ * sqrt(6)), or about 6.02 * n + 1.76 dB, where "n" is the number of output bits of the ADC.

Quantizer – A circuit that carries out the quantization process. Another name for an Analog-to-Digital Converter.

Reference Voltage – For an ADC, the reference voltage is the voltage against which the analog input or an ADC is compared to determine the ADC output code. For a DAC, the reference voltage is multiplied with the ratio of the DAC input code to its (full-scale code + 1) to determine its analog output.

Reflector – The longer elements of a "Yagi" antenna that reflect energy back to the driven element.

Resolution – A measure of how well the ADC input is "resolved", or how well the value of an LSB represents the analog input. Resolution is usually expressed in bits, and then indicates the number of bits available in the ADC output word.

The number of discrete output states or values of an ADC or a DAC, Can also be expressed in the number of digital bits in the output (for ADCs) or the input (for DACs).

Sampling Noise – The inherent noise of an ADC that comes from the steps in the transfer function.

Scale Factor – The effective multiplier of the analog reference voltage input to an ADC or DAC. This value is usually one, but can be any whole or fractional number.

Series Termination - Adding a resistor in series with a transmission line such that the driver output impedance plus the resistance of this external resistor is equal to the characteristic impedance of the transmission line.

ADC Glossary of Terms (3)

S/(N+D) – Signal-to-Noise Plus Distortion. See SINAD.

SINAD – Signal-to-Noise And Distortion ratio.A combination of the SNR and THD specifications, SINAD is defined as the rms value of the fundamental signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c. SINAD can be calculated from SNR and THD. Because it compares all undesired frequency components at the output with desired frequency. It is an overall measure of the dynamic performance of the ADC. SINAD is also known as SNDR, S/(N+D) and Signal-to-Noise Plus Distortion.

Skin Effect – The phenomenon by which high frequency current flow is restricted to the surface,or skin, of a conductor.

SNDR – Signal-to-Noise And Distortion Ratio. See SINAD.

SNR – Signal-to-Noise Ratio. The ratio of the power in the signal to the power in all other spectral components below ½ the sampling frequency, excluding harmonics and d.c.

Split Ground Plane – Concept where analog and digital grounds are in a single PCB layer and only connected at a single point.

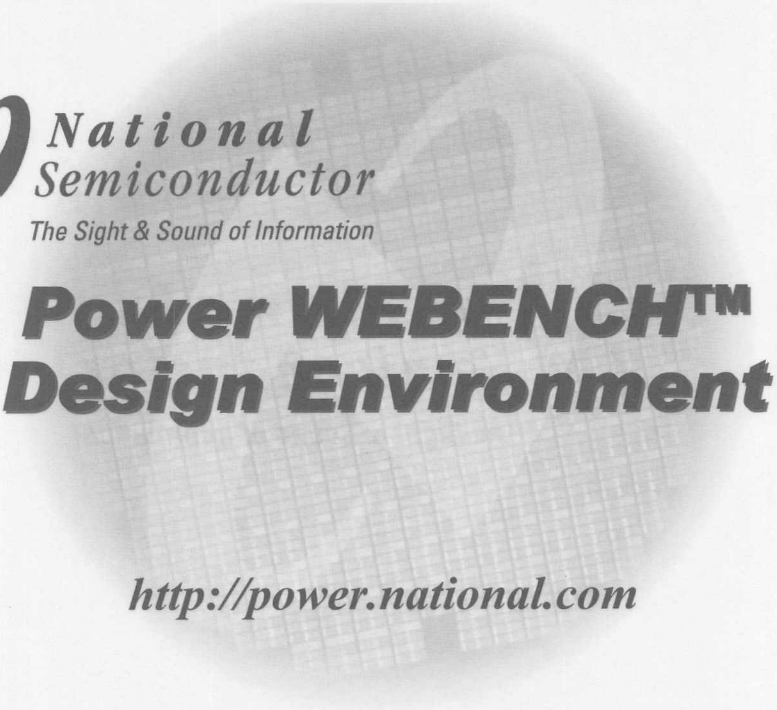
Substrate – The base semiconductor material upon with solid state devices are built. The substrate is resistive with a resistance that is on the order of a few Ohms.

THD – Total Harmonic Distortion. The ratio of the rms total of a specified number of harmonic components to the rms value of the output signal. National uses the first nine harmonics (f_2 through f_{10}).

Through Hole – The hole that goes through a printed circuit board to connect together lines and/or planes in two or more layers

V_{REF} – See “Reference Voltage”.

Z_O – The characteristic impedance of a transmission line



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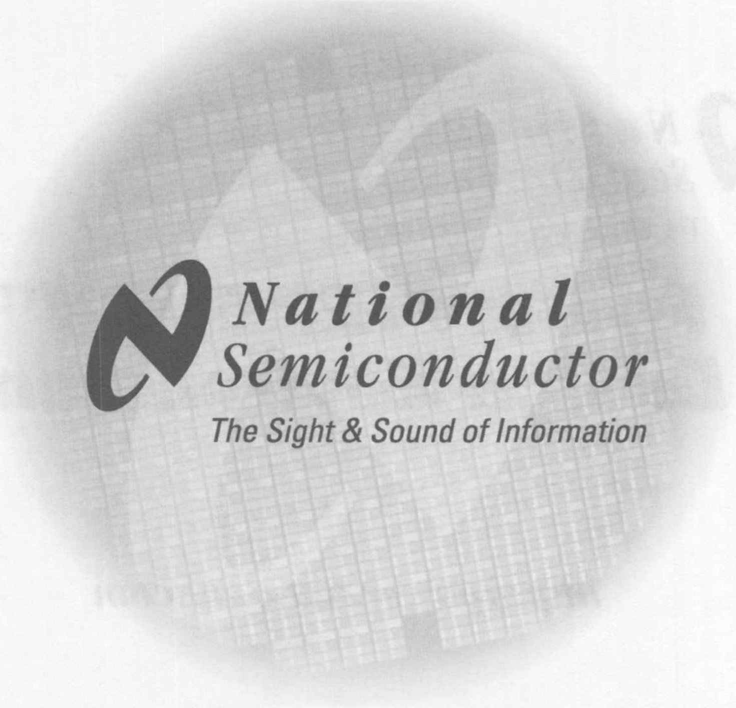
The Sight & Sound of Information

Power WEBENCH™ Design Environment

http://power.national.com



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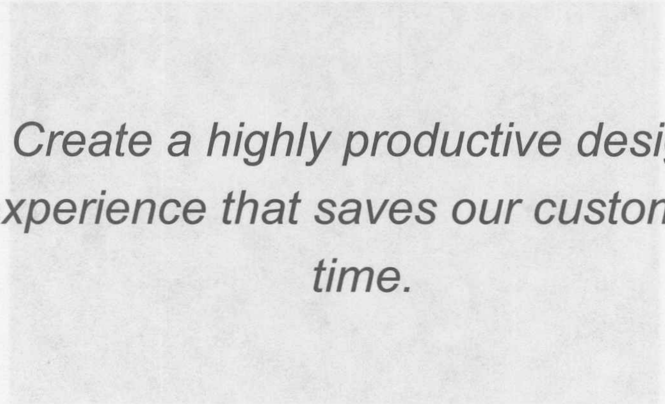
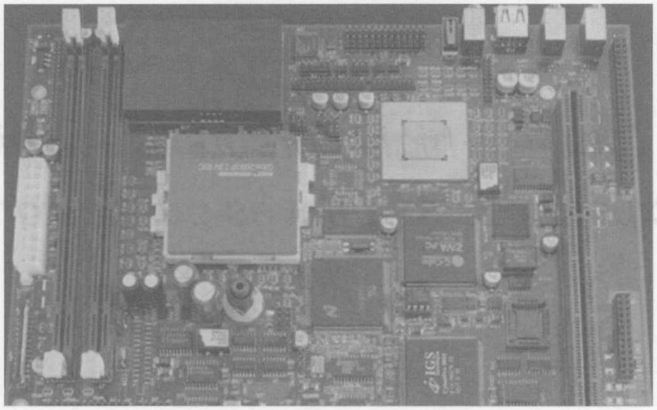
The Goal of WEBENCH.NATIONAL.COM



Create a highly productive design experience that saves our customers time.

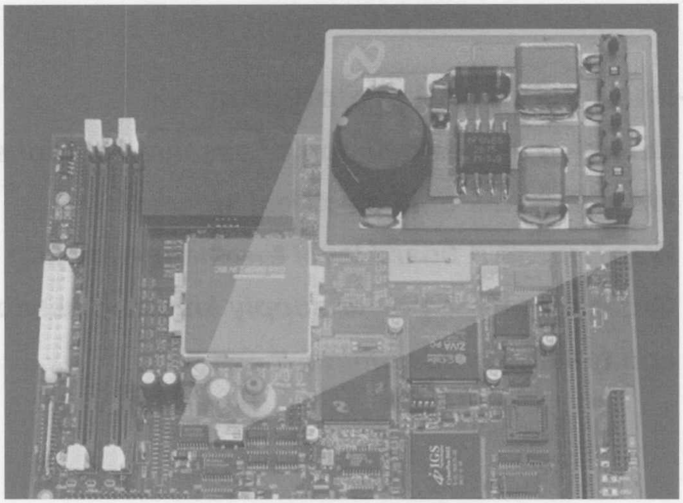
Before we created our web site, we defined our goal. In all of our development, we have kept this idea as our driving force: save our customers time.

Customers' Design Expertise and Time Goes Into the Main Board



Customers put their time and effort into the main board, and typically do not want to spend a lot of time designing a proprietary power supply circuit.

Objective: Get to This as Quickly as Possible



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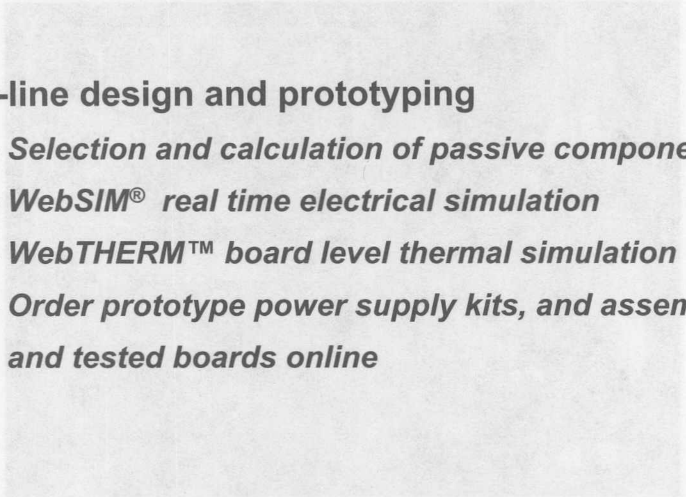
At POWER.NATIONAL.COM, National can provide the customer with a plug-in power supply design which is customized to the specifications of the customer's design.

WEBENCH™ Design Environment



On-line design and prototyping

- *Selection and calculation of passive components*
- *WebSIM® real time electrical simulation*
- *WebTHERM™ board level thermal simulation*
- *Order prototype power supply kits, and assembled and tested boards online*

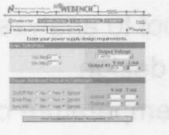
WEBENCH™ design tools are National's exciting on-line environment which saves our customers time in the design process

Power WEBENCH™ Design Benefits

- Save time by designing custom power supplies online, faster than ever
- WebSIM® is a powerful electrical simulation tool to analyze and optimize the electrical behavior of YOUR design
- WebTHERM™ provides visual results of the temperature of your custom board, as well as ways in which to lower it
- Order and purchase the following:
  - *Fully assembled and load tested custom board*
  - *Unassembled custom kit*
  - *National parts in volume*
  - *Free samples of National parts*
  - *Generic (non custom) evaluation board*

Power WEBENCH^{TM} Design
Four Easy Steps

1 Choose a Part

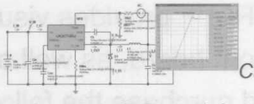


Enter Specifications

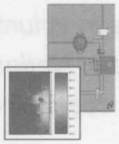
Select Part

2 Create a Design

3 Analyze a Design



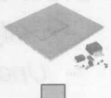
Generate Schematic/
Electrical Analysis



Generate Layout/
Thermal Analysis

4 Build It!

Custom Prototype Kit
Overnight



Prototype

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The Art of Analog 8

Available WebSIM® Devices Switchers

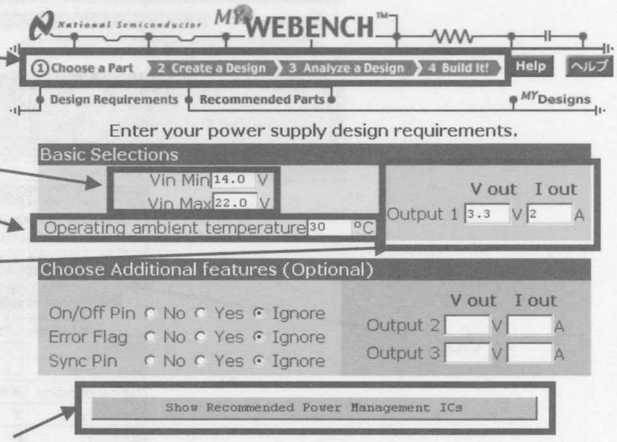
Device	Electrical Sim	Circ. Calc.	WebTHERM	Build It
LM2670,3,7,8,9	X	X	X	X
LM2671,2,4,5	X	X		
LM2595,6,8,9	X	X	X	X
LM2694,7,(+HV)	X	X		
LM2574,5,6, (+HV)	X			
LM2651,3	X			
LM2585,6,7,8, LM2577 Boost	X	X	X	X
LM2585,6,7,8, LM2577 Flyback	X	X		
LM2621 SEPIC, Boost	X			
LM3478/88 Boost	X			
LM5007	X			
LM5000	X			

Available WebSIM® devices – LDOs, Switched Capacitors

- Low Drop-out Linear Regulators
  - *Bipolar LDO: LP2978, LP2980, LP2981, LP2982, LP2985, LP2986, LP2987, LP2988,*
  - *Quasi-LDO: LM3480, LM3490*

- Switched-Capacitor Converters
  - *LM2660, LM2661, LM2662, LM2663, LM2664, LM2665, LM2681 (Doublers/Inverters)*
  - *LM3350, LM3351 (Fractional Converters 2/3 - 3/2)*

Enter Your Requirements



Follow the Steps

Enter Input Voltage Range

Enter temperature

Enter output voltage and maximum current

Go

Enter your power supply design requirements.

Vin Min 14.0 V

Vin Max 22.0 V

Operating ambient temperature 30 °C

	V out		I out	
Output 1	3.3	V	2	A
Output 2		V		A
Output 3		V		A

On/Off Pin ○ No ○ Yes ● Ignore

Error Flag ○ No ○ Yes ● Ignore

Sync Pin ○ No ○ Yes ● Ignore

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The Art of Analog 11

Now we will create a power supply design using power WEBENCH™.

On the very top of each screen in WEBENCH is a set of 4 buttons which tell the user which step the design process is in. These steps are:

Choose a Part,

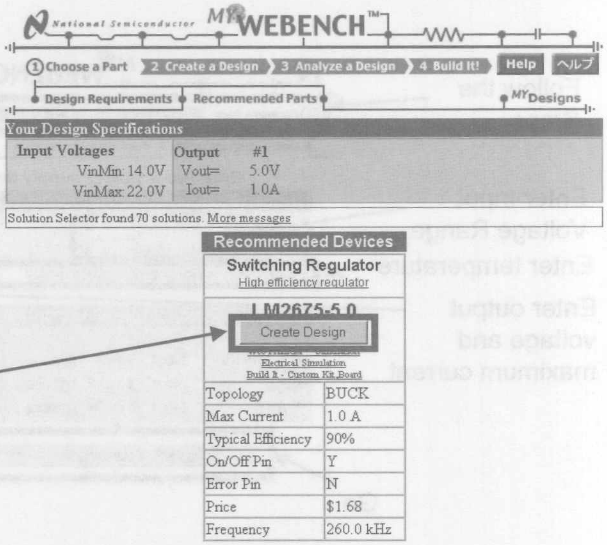
Create a Design,

Analyze a Design

Build It.

The first step is to enter the power supply design requirements in the Choose a Part screen. Simply enter the range for the input voltage (Vin), the desired output voltage and the output current. After entering the design specifications, press the button at the bottom of the screen to "Show Recommended Power Management ICs."

Show Recommended Parts



Your Design Specifications

Input Voltages	Output	#1
VinMin: 14.0V	Vout=	5.0V
VinMax: 22.0V	Iout=	1.0A

Solution Selector found 70 solutions. More messages

Recommended Devices

Switching Regulator

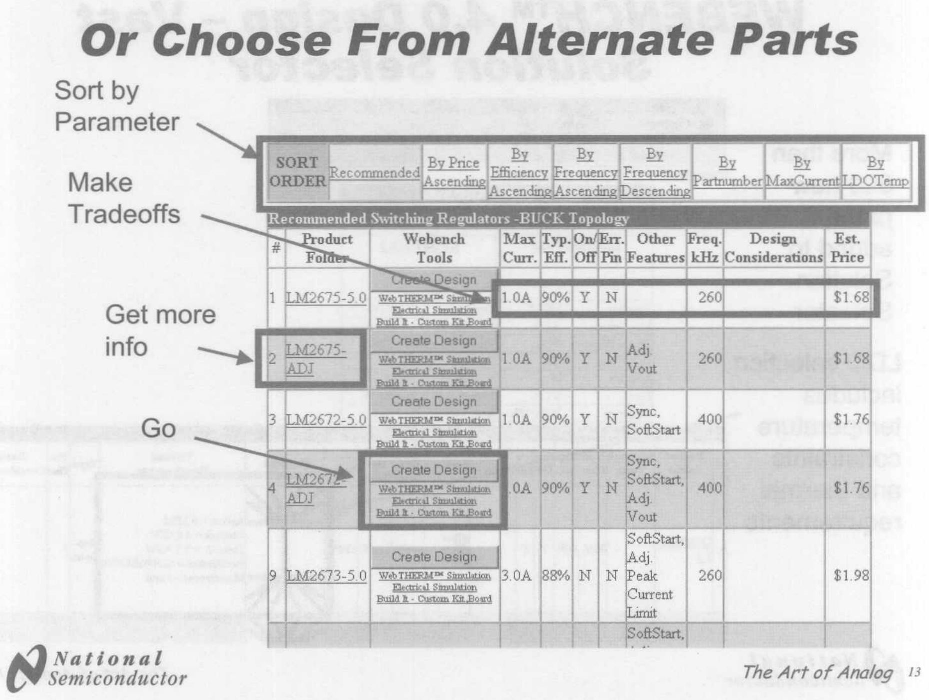
High efficiency regulator

LM2675-5.0

Topology	BUCK
Max Current	1.0 A
Typical Efficiency	90%
On/Off Pin	Y
Error Pin	N
Price	$1.68
Frequency	260.0 kHz

Go

On the "Recommended Parts" page, the recommended devices are shown at the top of the page. This may include a switching regulator, a linear regulator/LDO and/or a switched capacitor converter. If the recommended part is enabled for WEBENCH™, there will be a "create design" button below the part number. Clicking on that button will put you into the WEBENCH™ design environment.



Or Choose From Alternate Parts

Sort by Parameter

Make Tradeoffs

Get more info

Go

SORT ORDER	Recommended	By Price Ascending	By Efficiency Ascending	By Frequency Ascending	By Frequency Descending	By Partnumber	By MaxCurrent	By LDOTemp

Recommended Switching Regulators -BUCK Topology

#	Product Folder	Webench Tools	Max Curr.	Typ. Eff.	On/Off	Err. Pin	Other Features	Freq. kHz	Design Considerations	Est. Price
1	LM2675-5.0	Create Design WebTHERM™ Simulation Electrical Simulation Build It - Custom Kit Board	1.0A	90%	Y	N		260		$1.68
2	LM2675-ADJ	Create Design WebTHERM™ Simulation Electrical Simulation Build It - Custom Kit Board	1.0A	90%	Y	N	Adj. Vout	260		$1.68
3	LM2672-5.0	Create Design WebTHERM™ Simulation Electrical Simulation Build It - Custom Kit Board	1.0A	90%	Y	N	Sync, SoftStart	400		$1.76
4	LM2672-ADJ	Create Design WebTHERM™ Simulation Electrical Simulation Build It - Custom Kit Board	.0A	90%	Y	N	Sync, SoftStart, Adj. Vout	400		$1.76
9	LM2673-5.0	Create Design WebTHERM™ Simulation Electrical Simulation Build It - Custom Kit Board	3.0A	88%	N	N	SoftStart, Adj. Peak Current Limit	260		$1.98
							SoftStart,			

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The Art of Analog 13

Below the recommended parts is a sortable list of alternate devices which includes all Power Management products which address your power supply requirements. A number of useful parameters are displayed including efficiency and price which help you select the best part to meet your needs. If you desire more information about a device you can go to the device Product Folder, using the link in the left column of the display. Clicking on a sort link will re order the list based on parameters such as price, efficiency or frequency.

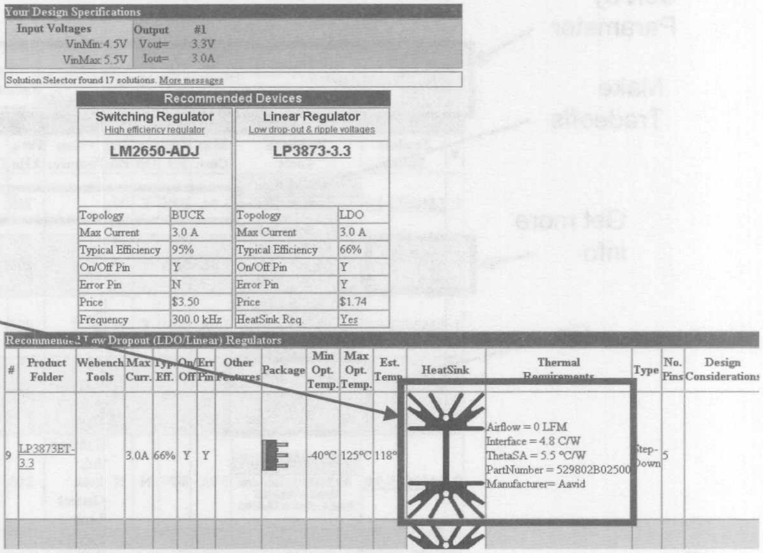
Text indicators below the Create Design buttons show whether the device is enabled for electrical simulation or WebTHERM™ simulation, meaning it can be simulated thermally. If the text indicator says "Build It Custom Kit", a custom prototype kit is available in the "Build It" step.

If you decide to use one of the alternate selections, click on the "Create Design" button next to the part name to have WEBENCH™ create your design in your personal workspace.

WEBENCH™ 4.0 Design – Vast Solution Selector

More than 500 new parts added to Solution Selector

LDO selection includes temperature constraints and thermal requirements



Your Design Specifications

Input Voltages	Output	#1
VinMin 4.5V	Vout=	3.3V
VinMax 5.5V	Iout=	3.0A

Solution Selector found 17 solutions. More messages

Recommended Devices

Switching Regulator High efficiency regulator		Linear Regulator Low drop-out & ripple voltages	
LM2650-ADJ		LP3873-3.3	
Topology	BUCK	Topology	LDO
Max Current	3.0 A	Max Current	3.0 A
Typical Efficiency	95%	Typical Efficiency	66%
On/Off Pin	Y	On/Off Pin	Y
Error Pin	N	Error Pin	Y
Price	$3.50	Price	$1.74
Frequency	300.0 kHz	HeatSink Req.	Yes

Recommended Low Dropout (LDO/Linear) Regulators

#	Product Folder	Webench Tools	Max Curr.	Typ. Eff.	On/Off	Err Pin	Other Features	Package	Min Opt. Temp.	Max Opt. Temp.	Est. Temp	HeatSink	Thermal Requirements	Type	No. Pins	Design Considerations
9	LP3873ET-3.3		3.0A	66%	Y	Y			-40°C	125°C	118°		Airflow = 0 LFM Interface = 4.8 C/W ThetaSA = 5.5 °C/W PartNumber = 529802B02500 Manufacturer= Aavid	Step-Down	5	

National Semiconductor

The Art of Analog 14

WEBENCH™ 4.0 design includes an upgraded solution selector which now includes over 500 new parts. Parts are listed even if they are not included in WEBENCH in order to give the widest possible selection. The selection criteria for LDOs (low dropout regulators) includes a thermal calculator which takes into account temperature constraints. If necessary, a heat sink, thermal grease and forced airflow will be recommended.

In this case, we've entered design parameters of:

Vin: 4.5 to 5.5 Volts

Vout: 3.3V

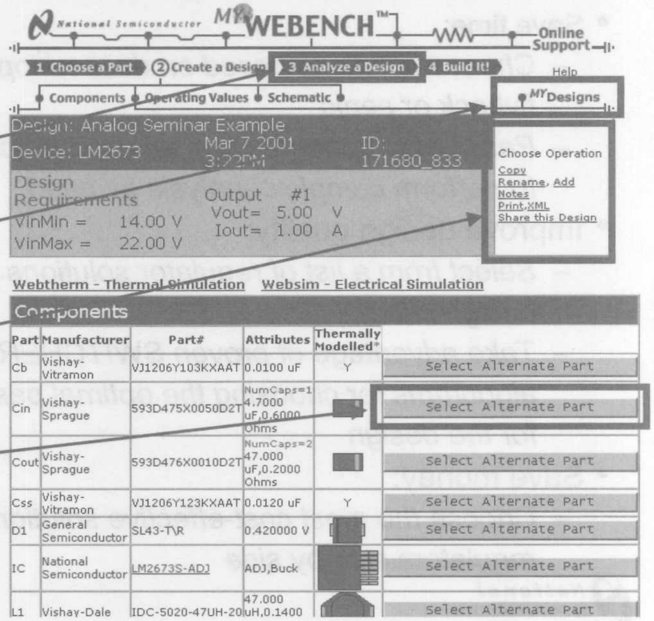
Iout: 3.0A

The results show a switcher and an LDO in the recommended parts list. However, the difference between the two options becomes apparent when we view the LDO details and find that there is a large heat sink required to keep the temperature below 125C.

Choose a Part - Benefits Experienced

- Save time:
  - *Choose solutions based on desired topology: buck, boost, flyback or sepic*
  - *Passive components are selected automatically – no need to perform complex analysis by hand*
- Improve design quality:
  - *Select from a list of regulator solutions appropriate for your design criteria*
  - *Take advantage of proven SWITCHERS MADE SIMPLE™ algorithms for choosing the optimal passive components for the design*
- Save money:
  - *Choose the most cost-effective solution by comparing regulators side by side*

Create a Design - View BOM



Design: Analog Seminar Example
Device: LM2673
Mar 7 2001
3:22PM
ID:
171680_833

Design Requirements
VinMin = 14.00 V
VinMax = 22.00 V

Output #1
Vout= 5.00 V
Iout= 1.00 A

Choose Operation
Copy
Rename, Add Notes
Print,XML
Share this Design

Webtherm - Thermal Simulation
Websim - Electrical Simulation

Components

Part	Manufacturer	Part#	Attributes	Thermally Modelled*	
Cb	Vishay-Vitramon	VJ1206Y103KXAAT	0.0100 uF	Y	Select Alternate Part
Cin	Vishay-Sprague	593D475X0050D2T	NumCaps=1 4.7000 uF,0.6000 Ohms		Select Alternate Part
Cout	Vishay-Sprague	593D476X0010D2T	NumCaps=2 47.000 uF,0.2000 Ohms		Select Alternate Part
Css	Vishay-Vitramon	VJ1206Y123KXAAT	0.0120 uF	Y	Select Alternate Part
D1	General Semiconductor	SL43-T\R	0.420000 V		Select Alternate Part
IC	National Semiconductor	LM2673S-ADJ	ADJ,Buck		Select Alternate Part
L1	Vishay-Dale	IDC-5020-47UH-20	47.000 uH,0.1400		Select Alternate Part

Click here to go to the next step

List all WEBENCH designs

File operations

Change passive components

National Semiconductor

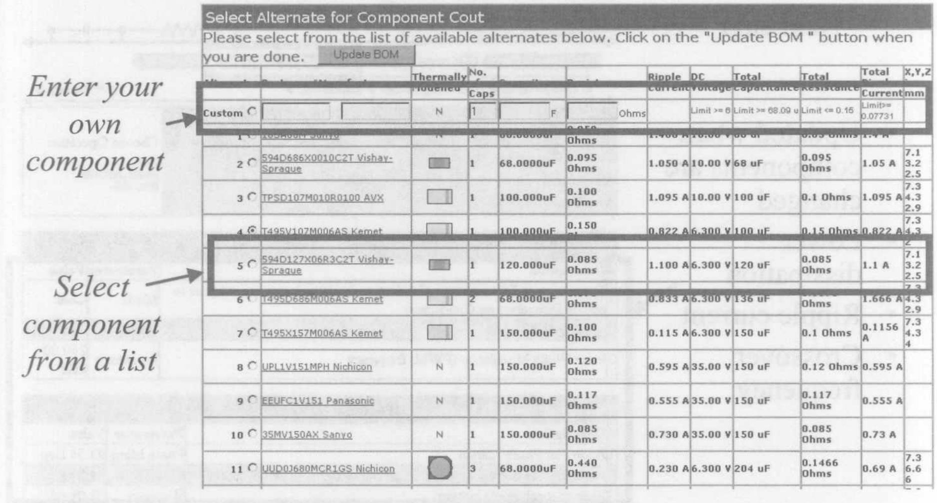
This is the "View Components" screen. It summarizes the design thus far, including the power supply requirements and the IC selected. In addition, the external components needed for the total solution are listed with manufacturer, part number, and key values. A top-view scaled drawing of each thermally modeled part is also shown. Parts which are not required by WebTHERM are indicated by a Y in the "Thermally Modeled" column. The component selection, as well as the operating value calculations, are done using the same algorithms as are used in Switchers Made Simple.

From here you can work with the design file name and information, view the operating values by clicking on the "Operating Values" tab, or select alternate component values for your design by clicking on any "Select Alternate Part" button. In each "Select Alternate Part" screen, it will list parameters for suggested alternate components including electrical, size and footprint data. You can also find out if the component is available for use in a custom prototype kit and how much the component costs. To get a quick view of the custom prototype availability, click on the "Build It" button.

To list all of your WEBENCH designs, click on the "MyDesigns" tab

To go to the next step and simulate the design using WebSIM™ or WebTHERM™, click on the 'Analyze a Design" button.

Select Alternate Part



Enter your own component

Select component from a list

Select Alternate for Component Cout

Please select from the list of available alternates below. Click on the "Update BOM " button when you are done. Update BOM

[illegible]	[illegible]	Thermally Modeled	No. of Caps	[illegible]	[illegible]	Ripple Current	DC Voltage	Total Capacitance	Total Resistance	Total [illegible] Current	X,Y,Z mm
Custom ○		N	1	F	Ohms		Limit >= 6	Limit >= 68.09 u	Limit <= 0.15	Limit>= 0.07731	
1 ○	[illegible] Sanyo	N	1	[illegible]	[illegible] Ohms	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
2 ○	594D686X0010C2T Vishay-Sprague	▬	1	68.0000uF	0.095 Ohms	1.050 A	10.00 V	68 uF	0.095 Ohms	1.05 A	7.1 3.2 2.5
3 ○	TPSD107M010R0100 AVX	▭	1	100.000uF	0.100 Ohms	1.095 A	10.00 V	100 uF	0.1 Ohms	1.095 A	7.3 4.3 2.9
4 ●	T495V107M006AS Kemet	▭	1	100.000uF	0.150 [illegible]	0.822 A	6.300 V	100 uF	0.15 Ohms	0.822 A	7.3 4.3 2
5 ○	594D127X06R3C2T Vishay-Sprague	▬	1	120.000uF	0.085 Ohms	1.100 A	6.300 V	120 uF	0.085 Ohms	1.1 A	7.1 3.2 2.5
6 ○	T495D686M006AS Kemet	▭	2	68.0000uF	[illegible] Ohms	0.833 A	6.300 V	136 uF	[illegible] Ohms	1.666 A	7.3 4.3 2.9
7 ○	T495X157M006AS Kemet	▭	1	150.000uF	0.100 Ohms	0.115 A	6.300 V	150 uF	0.1 Ohms	0.1156 A	7.3 4.3 4
8 ○	UPL1V151MPH Nichicon	N	1	150.000uF	0.120 Ohms	0.595 A	35.00 V	150 uF	0.12 Ohms	0.595 A	
9 ○	EEUFC1V151 Panasonic	N	1	150.000uF	0.117 Ohms	0.555 A	35.00 V	150 uF	0.117 Ohms	0.555 A	
10 ○	35MV150AX Sanyo	N	1	150.000uF	0.085 Ohms	0.730 A	35.00 V	150 uF	0.085 Ohms	0.73 A	
11 ○	UUD0J680MCR1GS Nichicon	●	3	68.0000uF	0.440 Ohms	0.230 A	6.300 V	204 uF	0.1466 Ohms	0.69 A	7.3 6.6 6

National Semiconductor

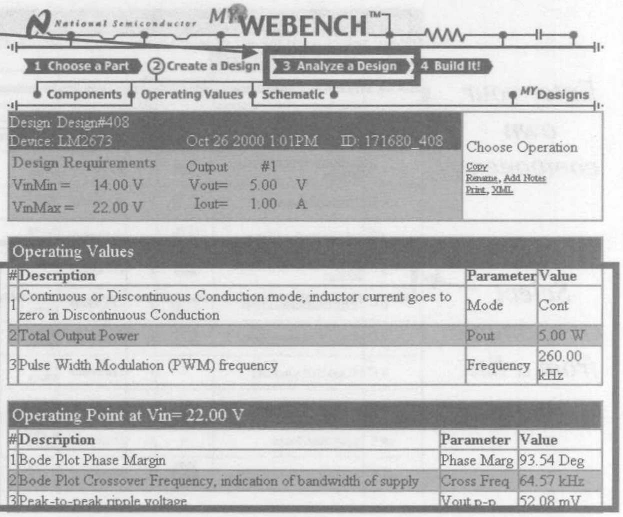
The Art of Analog 17

If you click on the "Choose Alternate Button" for the Cout component, the suggested alternative capacitors are listed, all appropriate for this power supply design. The limits for the capacitor parameters are listed in red at the top of the table. If another capacitor is desired that is not listed, it can be entered as custom (Be sure to click on the custom button if you want to enter custom values). Notice the ability to select multiple capacitors in parallel to reduce the equivalent series resistance and increase the capacitance.

Design – Operating Values

Next step

- Updated when components are changed
- Power dissipation
- Ripple current
- Crossover frequency



Design: Design#408
Device: LM2673 Oct 26 2000 1:01PM ID: 171680_408

Design Requirements
VinMin = 14.00 V
VinMax = 22.00 V

Output #1
Vout= 5.00 V
Iout= 1.00 A

Operating Values

#	Description	Parameter	Value
1	Continuous or Discontinuous Conduction mode, inductor current goes to zero in Discontinuous Conduction	Mode	Cont
2	Total Output Power	Pout	5.00 W
3	Pulse Width Modulation (PWM) frequency	Frequency	260.00 kHz

Operating Point at Vin= 22.00 V

#	Description	Parameter	Value
1	Bode Plot Phase Margin	Phase Marg	93.54 Deg
2	Bode Plot Crossover Frequency, indication of bandwidth of supply	Cross Freq	64.57 kHz
3	Peak-to-peak ripple voltage	Vout p-p	52.08 mV

The Operating Values page gives the result of calculations for the power supply design. These calculations were used in the selection of the design components, and are reported here to give an estimate of the circuit performance. In this example, the operating values provided are:

Bode Plot Phase Margin, Bode Plot Crossover Frequency

Steady State Efficiency, Continuous or Discontinuous Conduction mode

Total Output Power

IC Power Dissipation, Diode Power Dissipation

Input Capacitor Power Dissipation, Inductor Power Dissipation

Average input current, Input Capacitor RMS ripple current

IC Junction Temperature, IC Junction to Ambient Thermal Resistance

Vout p-p, Inductor ripple current, Output Capacitor RMS ripple current

Peak Current in IC for Steady-State Operating Point, IC Maximum rated peak current

Steady-State PWM Duty Cycle, Pulse Width Modulation (PWM) frequency

“View Components” will take you back to the previous page showing the components used in the design. If you change component values, the Operating Values will be updated.

For further investigation of the design, you can analyze it using the online WebSIM and WebTHERM™ simulation tools.

Create a Design - Benefits Experience

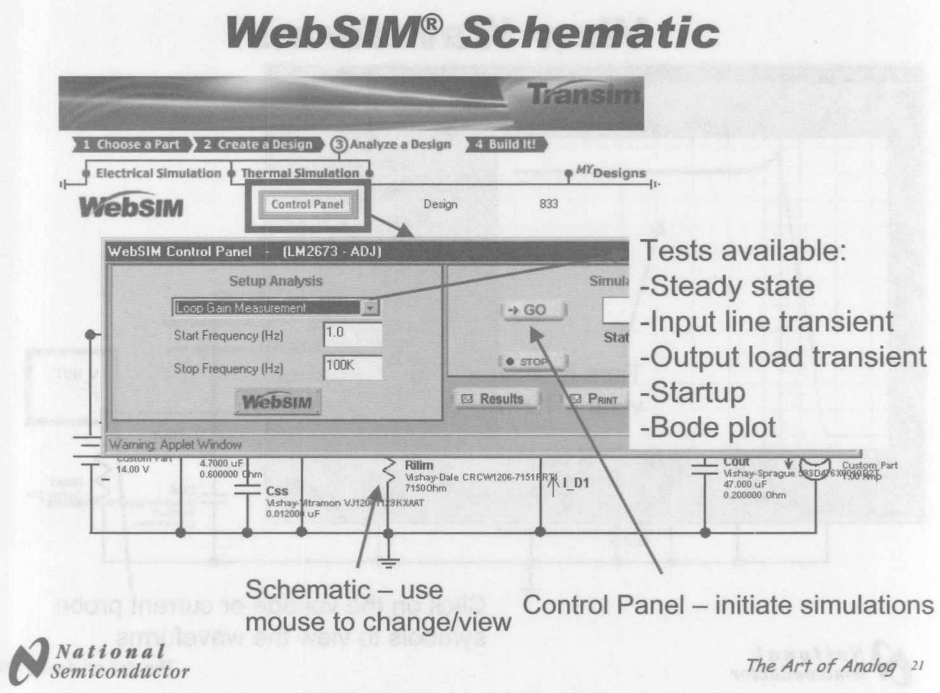
- Save time
  - *Select from lists of alternate passive components chosen specifically for your design criteria*
  - *Review the operating values for your design to determine maximum currents, power dissipation and key operating parameters*
  - *Share your design with co-workers or other stakeholders*
- Improve design quality
  - *Enter custom passive component values for components not in the WEBENCH™ database*
- Save money
  - *Compare passive components based on cost, size and performance*

What's Behind WebSIM®?

- **Developed in cooperation with Transim Corp.**
- **Large server runs simulation software**
- **Small java applet runs on user's browser**
  - ***Handles mouse movements and button clicks in real time***
- **Low bandwidth requirement**
- **WebSIM uses SIMPLIS for simulation of DC/DC and switched capacitor converters**
  - ***Simulation using piece-wise-linear models***
- **Berkeley SPICE used for linear regulators**

WebSIM® is a product of the Transim Technology Corp. Because WebSIM resides on a fast, high-powered server, the user does not need to have any special software loaded on his/her PC to be able to use it. The models and simulation engine software on the server are always up to date, so the user gets the most current information.

Only short data files are transferred between the user and the server across the Internet, so to set up and run a simulation is very fast. The simulations are also quick because the switching regulator and switched-capacitor models are in SIMPLIS, a Transim-proprietary modeling and simulation tool that is much faster than SPICE for switching circuits.



WebSIM® Schematic

WebSIM Control Panel - (LM2673 - ADJ)

Setup Analysis

Loop Gain Measurement

Start Frequency (Hz) 1.0

Stop Frequency (Hz) 100K

Tests available:
-Steady state
-Input line transient
-Output load transient
-Startup
-Bode plot

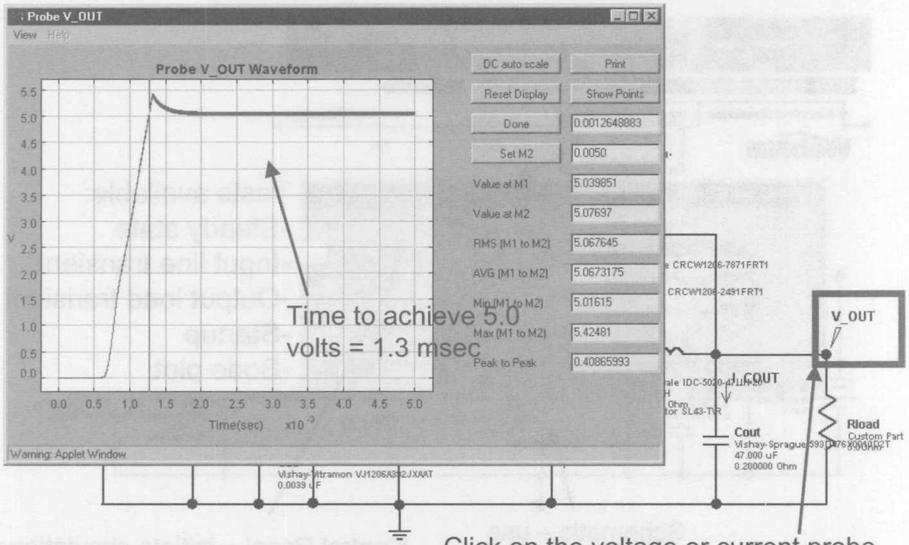
Schematic – use mouse to change/view

Control Panel – initiate simulations

National Semiconductor

Once in the "Analyze a Design" step, you may begin by using WebSIM™, by Transim Corporation, to do electrical simulations for your design. The schematic is generated by a Java applet that runs on the client browser. This allows the user to interact with the schematic in real time by rolling the mouse over parts or probe points in the circuit. The user can view component details by clicking on the corresponding symbol on the schematic. This brings up a window which allows the user to choose an alternate part if desired, or enter a custom value for that component. Set up simulations using the WebSIM™ control panel. If the control panel is closed, the user can reactivate it by pressing on the "Control Panel" button in the schematic. To run a simulation, click on the "Simulate" button in the Control Panel. Depending on the complexity of the simulation, results will be available typically in 15 to 30 seconds. After the simulation is complete, the current and voltage waveforms may be viewed by clicking on the appropriate probe symbol in the schematic. Several types of simulations may be run including start-up, input line transient, output load transient and steady state. A Bode plot, useful for confirming system stability can be obtained, by running the Loop Gain test.

View Waveforms



Done: 0.0012648883

Set M2: 0.0050

Value at M1: 5.039851

Value at M2: 5.07697

RMS (M1 to M2): 5.067645

AVG (M1 to M2): 5.0673175

Min (M1 to M2): 5.01615

Max (M1 to M2): 5.42481

Peak to Peak: 0.40865993

Time to achieve 5.0 volts = 1.3 msec

Click on the voltage or current probe symbols to view the waveforms

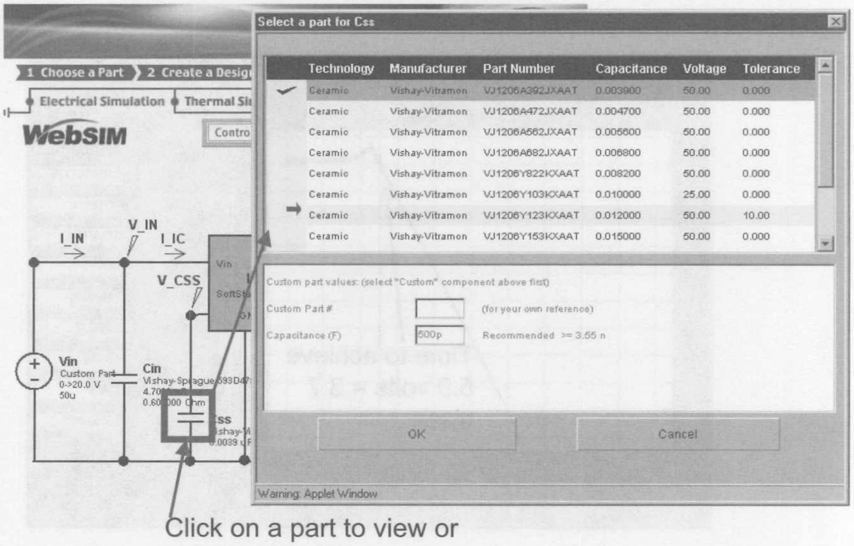
National Semiconductor

The Art of Analog 22

We will run a start-up test on this circuit to check the start-up time and determine if our soft start capacitor (Css) is correct for our design. For the start-up parameters we specify the input voltage going from 0 to 20V with a 50 usecond rise time. A simulation status window appears and indicates when the simulation is complete.

For the Startup test, as well as the transient and steady-state responses, two type of probes are available. The current probe allows the user to view the current through a component, and the voltage probe allows a look at the voltage with respect to ground. When we click on the Vout probe, we see the output waveform. Using the M1 measurement cursor, we see that it takes about 1.3 milliseconds to initially achieve 5 volts.

Changing Components



Select a part for Css

	Technology	Manufacturer	Part Number	Capacitance	Voltage	Tolerance
✓	Ceramic	Vishay-Vitramon	VJ1206A392JXAAT	0.003900	50.00	0.000
	Ceramic	Vishay-Vitramon	VJ1206A472JXAAT	0.004700	50.00	0.000
	Ceramic	Vishay-Vitramon	VJ1206A562JXAAT	0.005600	50.00	0.000
	Ceramic	Vishay-Vitramon	VJ1206A682JXAAT	0.006800	50.00	0.000
	Ceramic	Vishay-Vitramon	VJ1206Y822KXAAT	0.008200	50.00	0.000
	Ceramic	Vishay-Vitramon	VJ1206Y103KXAAT	0.010000	25.00	0.000
➡	Ceramic	Vishay-Vitramon	VJ1206Y123KXAAT	0.012000	50.00	10.00
	Ceramic	Vishay-Vitramon	VJ1206Y153KXAAT	0.015000	50.00	0.000

Custom part values: (select "Custom" component above first)

Custom Part # (for your own reference)

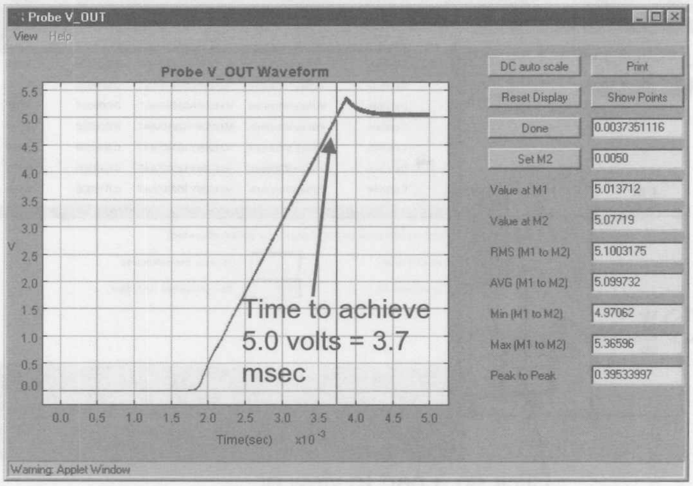
Capacitance (F) 500p Recommended >= 3.55 n

Warning: Applet Window

Click on a part to view or change it

We change the soft start capacitor (Css) from 3.9 nF to 12 nF and run another simulation.

Vout Waveform After Css Change

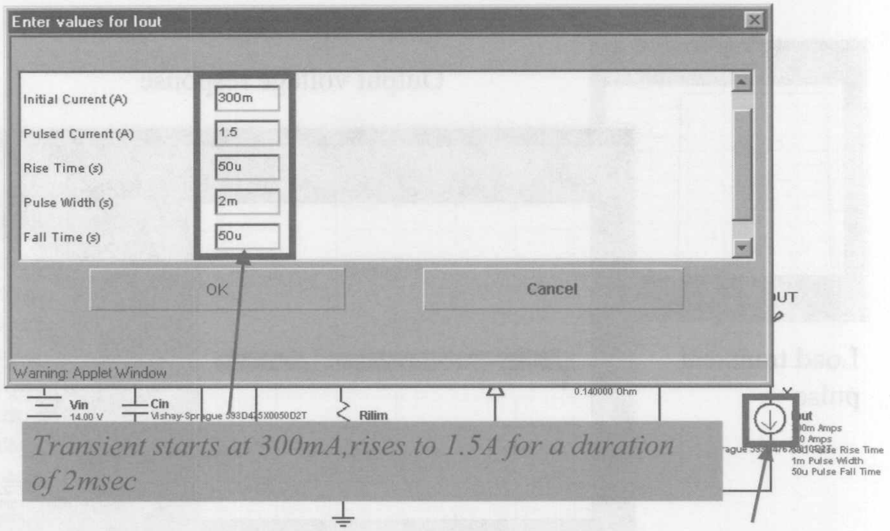


Done	0.0037351116
Set M2	0.0050
Value at M1	5.013712
Value at M2	5.07719
RMS (M1 to M2)	5.1003175
AVG (M1 to M2)	5.099732
Min (M1 to M2)	4.97062
Max (M1 to M2)	5.36596
Peak to Peak	0.39533997

Time to achieve 5.0 volts = 3.7 msec

Then we see that the time to reach 5 volts has increased from 1.3 milliseconds to 3.7 milliseconds.

Load Transient Test



Enter values for Iout

Initial Current (A): 300m

Pulsed Current (A): 1.5

Rise Time (s): 50u

Pulse Width (s): 2m

Fall Time (s): 50u

Warning: Applet Window

Transient starts at 300mA,rises to 1.5A for a duration of 2msec

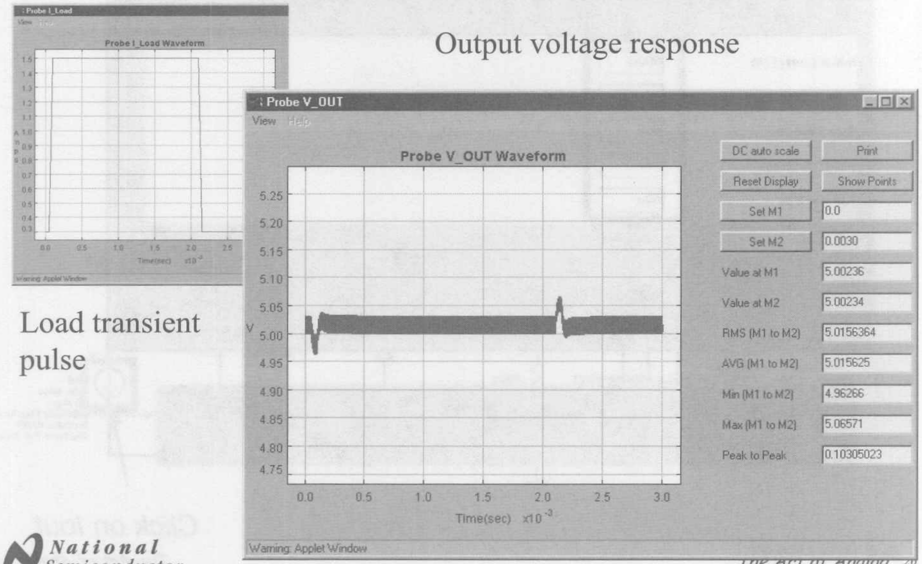
Click on Iout

National Semiconductor

The Art of Analog 25

To run the Load Transient Response test, it is useful to check the load transient settings and adjust them, if necessary. The settings include the initial current level, the maximum current level, rise time of the pulse, the duration (pulse width), and the fall time. Here we have adjusted the load transient to step from 300mA to 1.5A, with a duration of 2msec. The rise and fall times are unchanged at 50us. In the Control Panel, the overall simulation time is set to 3msec.

Vout for Load Transient



Set M1: 0.0
Set M2: 0.0030
Value at M1: 5.00236
Value at M2: 5.00234
RMS (M1 to M2): 5.0156364
AVG (M1 to M2): 5.015625
Min (M1 to M2): 4.96266
Max (M1 to M2): 5.06571
Peak to Peak: 0.10305023

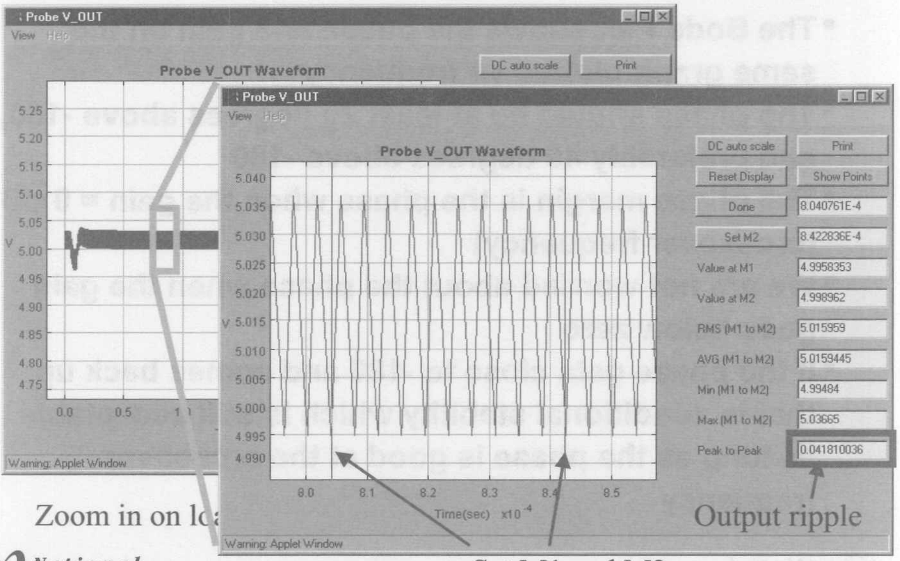
Output voltage response

Load transient pulse

National Semiconductor

After running the test, and get the message "Simulation Completed"; you may view the results now, we click on the output voltage probe, and see the waveform there due to the load transient. It is reasonably well-damped, with just one cycle of ringing.

Output Ripple Voltage



Done: 8.040761E-4

Set M2: 8.422836E-4

Value at M1: 4.9958353

Value at M2: 4.998962

RMS (M1 to M2): 5.015959

AVG (M1 to M2): 5.0159445

Min (M1 to M2): 4.99484

Max (M1 to M2): 5.03665

Peak to Peak: 0.041810036

Zoom in on lo

Set M1 and M2

Output ripple

National Semiconductor

The Art of Analog 27

We can zoom in on a section of the waveform, and see the output voltage ripple due to the switching action of the regulator. In the zoomed-in view, we can take advantage of the built-in calculator to measure the peak-to-peak output voltage ripple at full load, a little less than 42 mV.

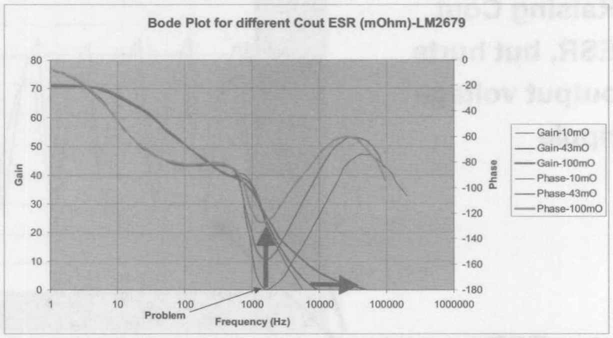
WebSIM® Bode Plots

- The Bode Plot shows the phase and gain on the same graph plotted vs frequency
- The phase should be at least 25 degrees above -180, and preferably 45 degrees above -180
- The phase margin is the phase when the gain = 0 dB (crossover frequency)
- We are not worried about the phase when the gain goes below zero
- If the phase gets close to -180 and comes back up, that is conditional stability which is still acceptable as long as the phase is good at the crossover frequency

The Bode plot is an important tool to examine the stability of a design. Bode plots are easy to get using WebSIM. Simply run a loop gain simulation, and the Bode plot will appear. If the Bode plot window gets closed, you can make it reappear by clicking on the "results" button in the control panel.

Effect of Cout ESR on Stability

- **Raising Cout ESR helps conditional stability issues**



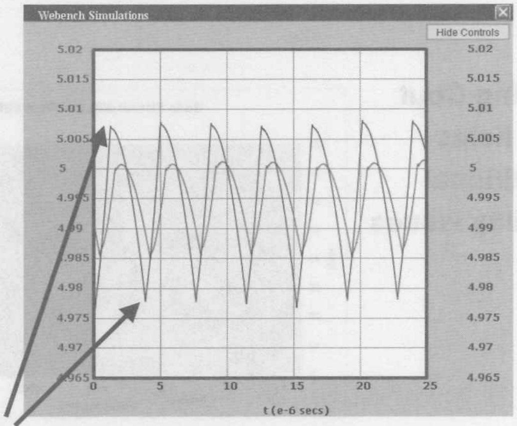
Higher ESR moves phase up at lower frequencies

Higher ESR increases crossover frequency

This is a plot of several WebSIM® Bode Plots for different output capacitor ESRs for a design using an LM2679 switching regulator. The phase is plotted in blue and the gain in red. All the runs show a dip in the phase at about 1500Hz. This is called conditional stability. The phase increases at higher frequencies and then drops again above the crossover frequency. We see from the plot that we can improve the conditional stability issue by raising the ESR of the output capacitor. This also increases the crossover frequency and bandwidth.

Effect of Cout ESR on Vout Ripple

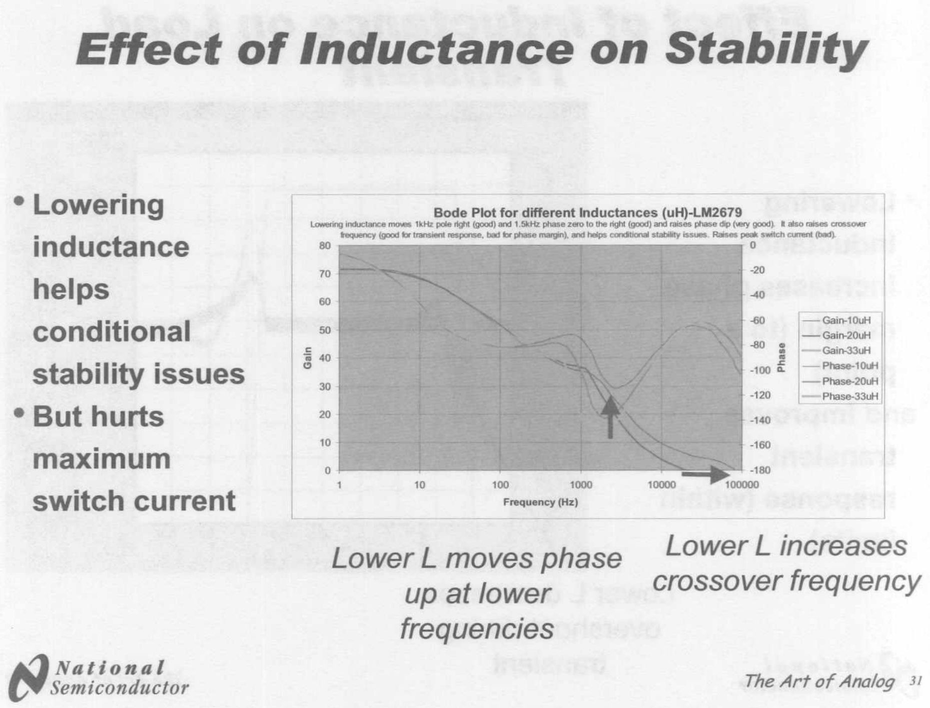
- Raising Cout ESR, but hurts output voltage ripple



Higher ESR increases ripple on output voltage

National Semiconductor

The other effect of changing the output capacitor ESR is that the output voltage ripple increases as the output capacitor ESR goes up. You can use the WEBENCH™ electrical simulator to examine the output voltage waveform after the Cout ESR is adjusted to make sure that the voltage ripple is within your spec.



Effect of Inductance on Stability

- Lowering inductance helps conditional stability issues
- But hurts maximum switch current

Bode Plot for different Inductances (uH)-LM2679

Lowering inductance moves 1kHz pole right (good) and 1.5kHz phase zero to the right (good) and raises phase dip (very good). It also raises crossover frequency (good for transient response, bad for phase margin), and helps conditional stability issues. Raises peak switch current (bad).

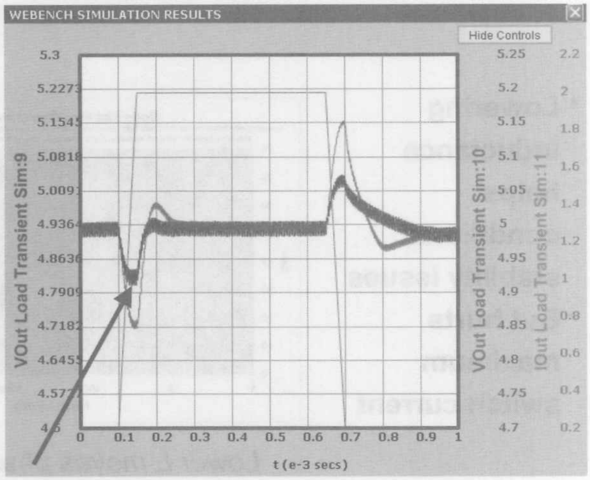
Lower L moves phase up at lower frequencies

Lower L increases crossover frequency

National Semiconductor

This is a plot of several WebSIM® bode plots for different inductances for the same LM2679 design. The phase is again plotted in blue and the gain in red. All the runs show a dip in the phase at about 1600 - 2700Hz. The phase can be raised at the lower frequencies by decreasing the inductance. However, this may cause a problem with the maximum switch current. You can use WebSIM to examine the switch current waveform (the current probe which is coming out of the regulator into the inductor) after you adjust the inductor to make sure that the switch current does not exceed the rating for the voltage regulator.

Effect of Inductance on Load Transient



- **Lowering inductance increases phase margin (to a point)**

and improves transient response (within limits)

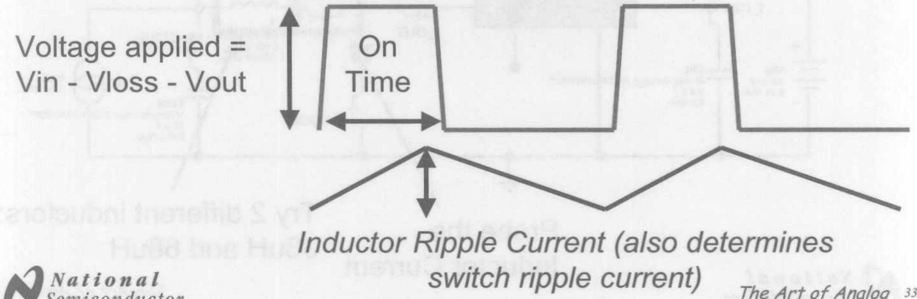
Lower L decreases overshoot during transient

National Semiconductor

The Vout load transient response is plotted for several different inductances. The blue plot is for 33uH and the red plot is for 68uH. For this design, the 33uH L value, which corresponds to higher phase margin on the Bode Plot, results in less excursion during the load transitions. However, when we go down to 5uH, the design goes into discontinuous mode which causes the current to go higher when the switch is on. This results in a large output voltage ripple. In this case, the device is also put into current limit. We will explore this relationship further in the next slides.

Now Does the Inductor Affect Peak Current?

- **Basic inductor Equation: V = L di/dt**
- **di = (1/L) * voltage applied across inductor * time voltage is on = ILpp**
- **On time = duty cycle * 1/frequency**
  - ***Higher switching frequency = less on time***
- **Ipeak = ILavg + ½ ILpp**



Voltage applied =
Vin - Vloss - Vout

On
Time

Inductor Ripple Current (also determines switch ripple current)

The peak inductor current (and peak switch current) is a function of the average output current and the inductor ripple current. The peak inductor current is:

ILaverage + 1/2 ILpp (the inductor ripple current) The average inductor current is:

For Buck: ILaverage = Iout

For Boost: ILaverage = Iout/(1-DC) where DC = duty cycle

DC = (Vout-Vin+Vdiode+ILavg*DCR)/(Vout - Vswitch + Vdiode)

Higher DCR means higher duty cycle and higher average inductor current

The inductor ripple current is determined by the basic inductor equation:

V = L dI/dt

di = V/L dt

Peak to peak inductor current (inductor ripple current) = Voltage applied across the inductor/L * time during which voltage is applied to the inductor.

When the switch is closed we have:

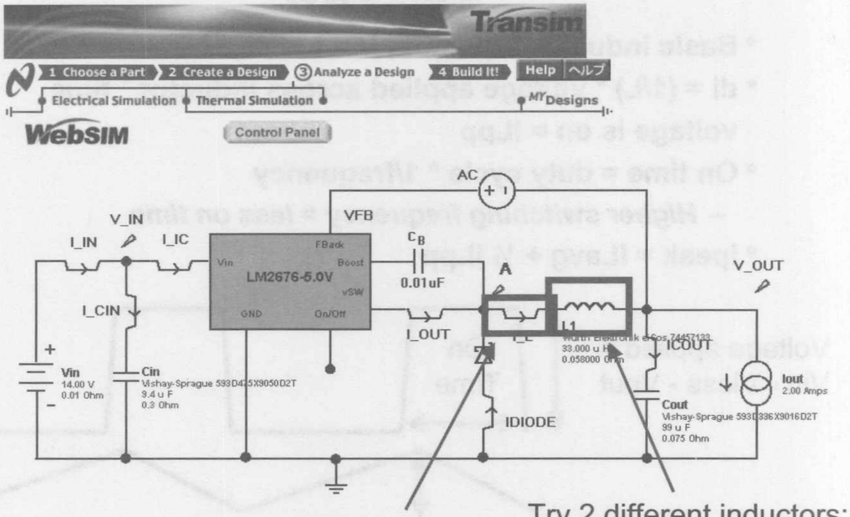
For Buck: ILpp = (Vin - Vswitchingloss - ILavg*DCR - Vout)/L * Ton

For Boost: ILpp = (Vin - Vswitchingloss - ILavg*DCR)/L * Ton

Longer ON times and lower inductance values mean more inductor ripple current and higher peak current.

Note: When creating a design, the rule for sizing an inductor is to try for +/- 15% inductor ripple current.

Try Different Components



Probe the Inductor Current

Try 2 different inductors: 33uH and 68uH

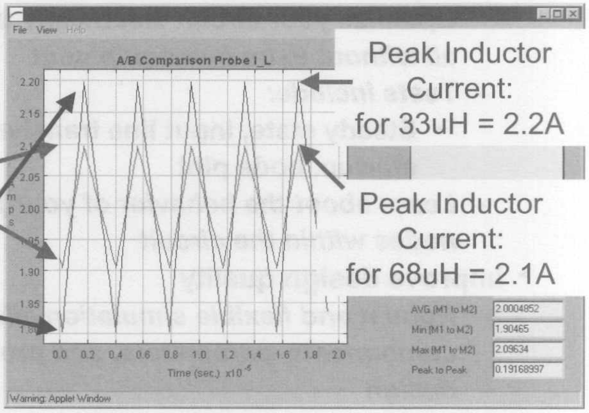
National Semiconductor

The Art of Analog 34

We will investigate the effect of inductance on inductor/switch ripple current using WebSIM®. First we try a steady-state simulation using a 33uH inductor. We can view the inductor current by clicking on the "Inductor Probe Symbol". We can temporarily store one set of waveform data by clicking on the "data/store menu" choice in the waveform viewer. Next, we change the inductor to 68uH and run another simulation. We can compare the data with the previous simulation by clicking on the "data/retrieve menu" option in the waveform viewer.

Effect of Inductance on Inductor/Switch Ripple Current

68uH
$2.47



AVG (M1 to M2) 2.0004852
Min (M1 to M2) 1.90465
Max (M1 to M2) 2.09634
Peak to Peak 0.19168997

Peak-to-Peak
Inductor Current:
for 68uH = .20A

Peak-to-Peak
Inductor Current:
for 33uH = .39A

Peak Inductor
Current:
for 33uH = 2.2A

Peak Inductor
Current:
for 68uH = 2.1A

33uH
$0.84

We see that the peak-to-peak inductor current, ILpp, is reduced from .39A down to .2A by increasing the inductor from 33uH to 68uH. We also see that since changing the inductor has negligible effect on the average output current, the peak inductor current was also reduced from 2.2A down to 2.1A. This follows since:

ILpeak = ILaverage + ½ ILpp where ILaverage = Iout (neglecting the effect of inductor DC resistance).

However, increasing the inductance can result in a significantly larger footprint at more cost.

Benefits Experienced - WebSIM®

- Save time:
  - *Optimize your circuit electrically up front before you build, all without extra test equipment*
  - *Tests include:*
    - Steady state, input line transient, output load transient, startup, bode plot
  - *Learn about the behavior of your power supply by probing nodes within the circuit*
- Improve design quality
  - *Robust and flexible simulation allows you to change components, parameters, and probe nodes to optimize your design*
- Save money
  - *Avoid costly prototype iterations by optimizing in advance*

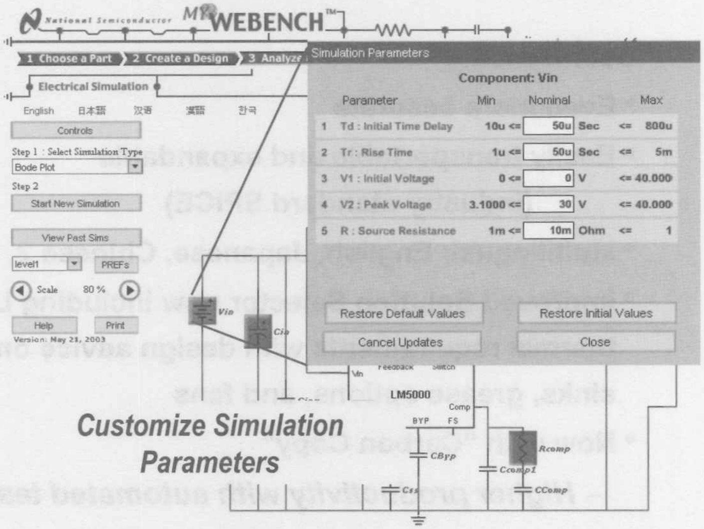
New In WEBENCH™ 4.0 Design Environment

User Benefits

- Even more accurate
- Easily transportable and expandable (industry standard SPICE)
- Multilingual: English, Japanese, Chinese 2, Korean
- Improved Solution Selector now including LDO thermal requirements with design advice on heat sinks, grease options, and fans
- Now with "Carbon Copy"
  - *Higher productivity with automated test suites*

National Semiconductor

WEBENCH™ 4.0 Design – with SPICE



Step 1 : Select Simulation Type: Bode Plot

Step 2

level1

Scale 80 %

Version: May 21, 2003

Simulation Parameters

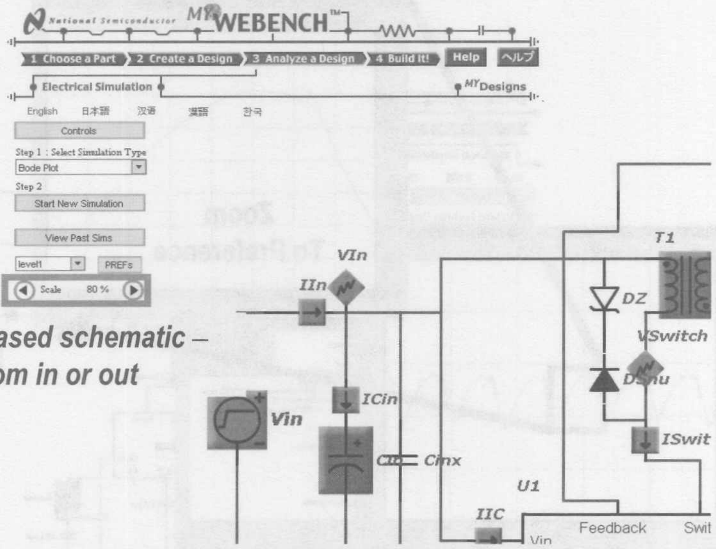
Component: Vin

	Parameter	Min	Nominal			Max
1	Td : Initial Time Delay	10u <=	50u	Sec	<=	800u
2	Tr : Rise Time	1u <=	50u	Sec	<=	5m
3	V1 : Initial Voltage	0 <=	0	V	<=	40.000
4	V2 : Peak Voltage	3.1000 <=	30	V	<=	40.000
5	R : Source Resistance	1m <=	10m	Ohm	<=	1

Customize Simulation Parameters

WEBENCH™ 4.0 has a new GUI that incorporates Macromedia Flash for better compatibility.

WEBENCH™ 4.0 Design New Interface



Step 1 : Select Simulation Type: Bode Plot

Step 2

level1

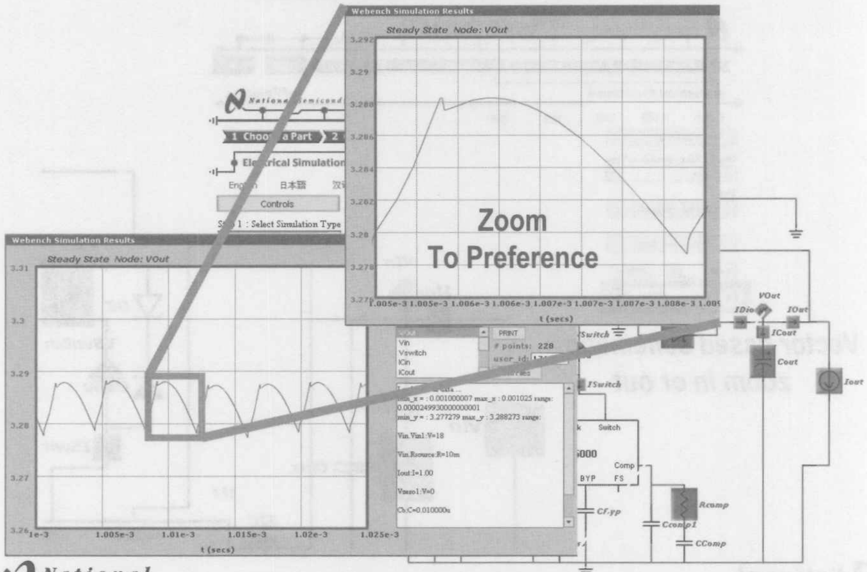
Scale 80 %

Vector based schematic – zoom in or out

National Semiconductor

In WEBENCH™ 4.0 schematic drawings are vector based which allows zoom and scroll.

WEBENCH™ 4.0 Design Waveform Viewer



```
min_x = : 0.001000007 max_x : 0.001025 range:
0.000024993000000001
min_y = : 3.277279 max_y : 3.288273 range:

Vin.Vin1:V=18

Vin.Rsource:R=10m

Iout:I=1.00

Vzero1:V=0

Cb:C=0.010000u
```

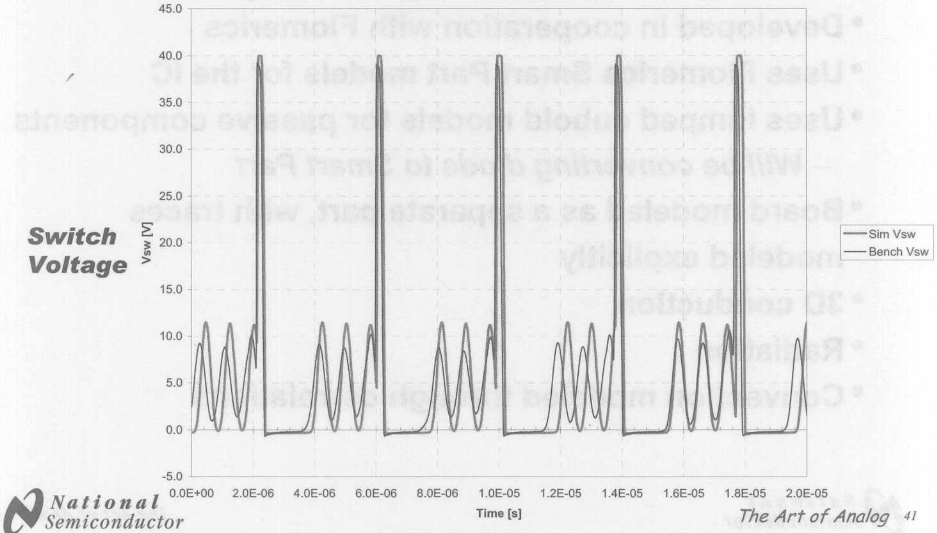
National Semiconductor

The Art of Analog 40

The new WEBENCH™ 4.0 electrical simulator waveform viewer allows the user to view waveforms in real time. The data can also be downloaded to the user's computer for off line use in reports or data analysis.

WEBENCH™ 4.0 Design – Accuracy

Plot of Bench data (lower amplitude) and Simulation Data (higher)
Showing Accurate Depiction of Discontinuous Mode



National Semiconductor

The Art of Analog 41

WEBENCH™ 4.0 has improved accuracy in electrical simulation. The use of Spice for the simulation engine has enabled this to happen. More accurate models for the output capacitor and diode have also been implemented along with the new Spice IC models. Extensive correlations with bench data have been performed in order to fine-tune the models and assure accuracy.

What's Behind WebTHERM™?

- Developed in cooperation with Flomerics
- Uses Flomerics Smart Part models for the IC
- Uses lumped cuboid models for passive components
  - *Will be converting diode to Smart Part*
- Board modeled as a separate part, with traces modeled explicitly
- 3D conduction
- Radiation
- Convection modeled through correlations

WebTHERM™ uses two types of models for electrical simulation. For the IC, WebTHERM uses Flomerics Smart Part models which are highly detailed and based on the internal construction of the parts. For other passive components, lumped cuboid models are used which assume the power is distributed evenly across the cubic volume of the component. Since the passive parts do not generate a lot of heat in these designs, this type of model is appropriate. The board traces are modeled explicitly to accurately portray how heat is transferred over the copper.

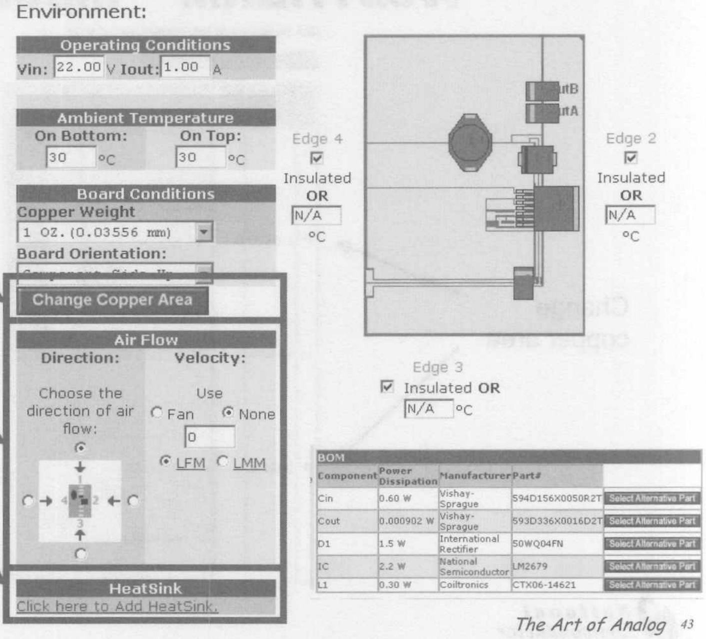
The simulation engine uses full 3-D conduction and radiation solvers. Convection (including air flow) is modeled through correlations, this is because full CFD simulations for air flow require extended simulation times which are too long for WEBENCH™.

WebTHERM™ Inputs

Change copper area

Change air velocity and direction

Add heat sink



Environment:

Operating Conditions

Vin: 22.00 V Iout: 1.00 A

Ambient Temperature

On Bottom: 30 °C

On Top: 30 °C

Board Conditions

Copper Weight: 1 oz.(0.03556 mm)

Board Orientation:

Change Copper Area

Air Flow

Direction: Choose the direction of air flow:

Velocity: Use ○ Fan ● None

0

● LFM ○ LMM

HeatSink

Click here to Add HeatSink.

Edge 4 ☑ Insulated OR N/A °C

Edge 2 ☑ Insulated OR N/A °C

Edge 3 ☑ Insulated OR N/A °C

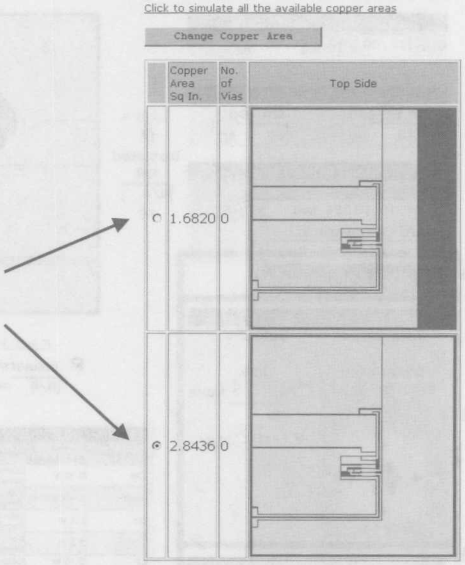
BOM				
Component	Power Dissipation	Manufacturer	Part#	
Cin	0.60 W	Vishay-Sprague	594D156X0050R2T	Select Alternative Part
Cout	0.000902 W	Vishay-Sprague	593D336X0016D2T	Select Alternative Part
D1	1.5 W	International Rectifier	50WQ04FN	Select Alternative Part
IC	2.2 W	National Semiconductor	LM2679	Select Alternative Part
L1	0.30 W	Coiltronics	CTX06-14621	Select Alternative Part

National Semiconductor

The Art of Analog 43

This is the initial parameter entry screen of WebTHERM™ where you can view the reference printed-circuit-board layout, adjust the air flow velocity, change the copper area or thickness, adjust the top and bottom ambient temperatures, and specify the board edge boundary temperatures, either insulated or fixed. In addition you can enter the orientation of the board, and/or enter comments about the design. Here, we are looking at a TO-263 surface mount design. To change the copper area, click on the red "Change Copper Area button"

WebTHERM™ Inputs



Click to simulate all the available copper areas

	Copper Area Sq In.	No. of Vias	Top Side
○	1.6820	0	
●	2.8436	0	

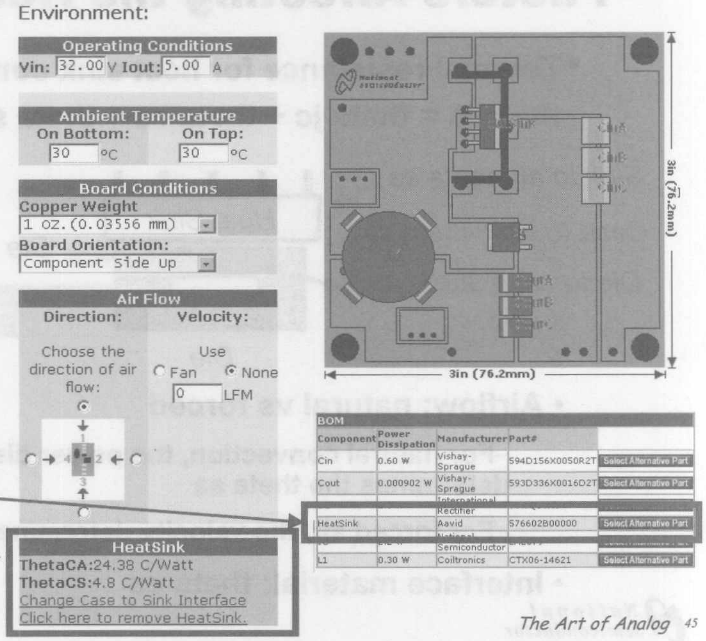
Change copper area

National Semiconductor

The Art of Analog 44

To change the copper area on a TO-263 surface mount design, simply select the desired board layout and click on the gray "Change Copper Area" button. You can also simulate all the copper areas at once by clicking on the "Simulate All Available Copper Areas" link at the top of the page.

WebTHERM™ Inputs



Environment:

Operating Conditions

Vin: 32.00 V Iout: 5.00 A

Ambient Temperature

On Bottom: 30 °C

On Top: 30 °C

Board Conditions

Copper Weight: 1 oz.(0.03556 mm)

Board Orientation: Component Side Up

Air Flow

Direction: Choose the direction of air flow:

Velocity: Use ○ Fan ● None

0 LFM

HeatSink

ThetaCA: 24.38 C/Watt

ThetaCS: 4.8 C/Watt

Change Case to Sink Interface

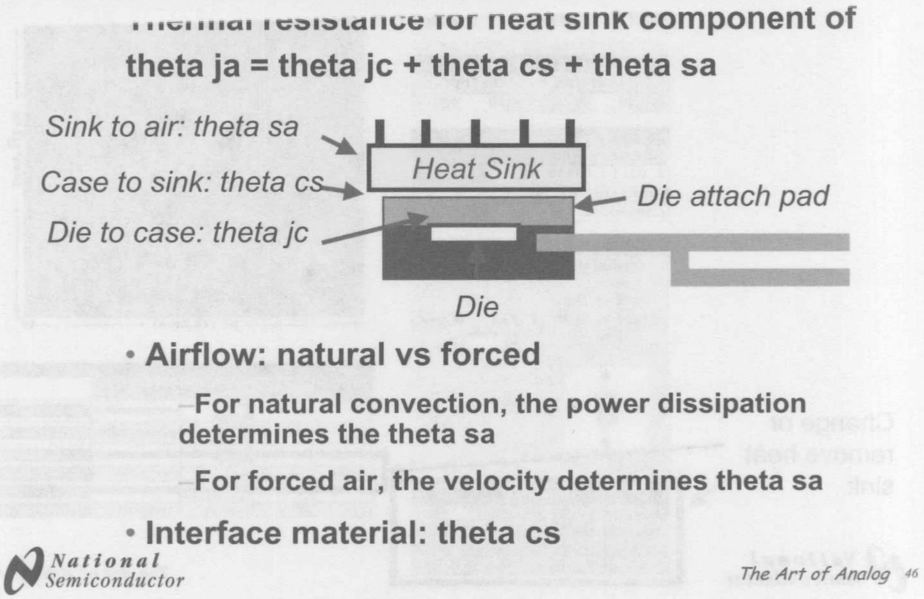
Click here to remove HeatSink.

BOM

Component	Power Dissipation	Manufacturer	Part#	
Cin	0.60 W	Vishay-Sprague	594D156X0050R2T	Select Alternative Part
Cout	0.000902 W	Vishay-Sprague	593D336X0016D2T	Select Alternative Part
[illegible]	[illegible]	International Rectifier	[illegible]	[illegible]
HeatSink		Aavid	576602B00000	Select Alternative Part
[illegible]	[illegible]	National Semiconductor	[illegible]	[illegible]
L1	0.30 W	Coiltronics	CTX06-14621	Select Alternative Part

Change or remove heat sink

Here is the screen showing the parameters for a heat sink design. This is similar to the surface mount version except it has added links to change the heat sink parameters.



Thermal resistance for heat sink component of

theta ja = theta jc + theta cs + theta sa

Sink to air: theta sa

Case to sink: theta cs

Die to case: theta jc

- **Airflow: natural vs forced**
  - **For natural convection, the power dissipation determines the theta sa**
  - **For forced air, the velocity determines theta sa**
- **Interface material: theta cs**

National Semiconductor

The Art of Analog 46

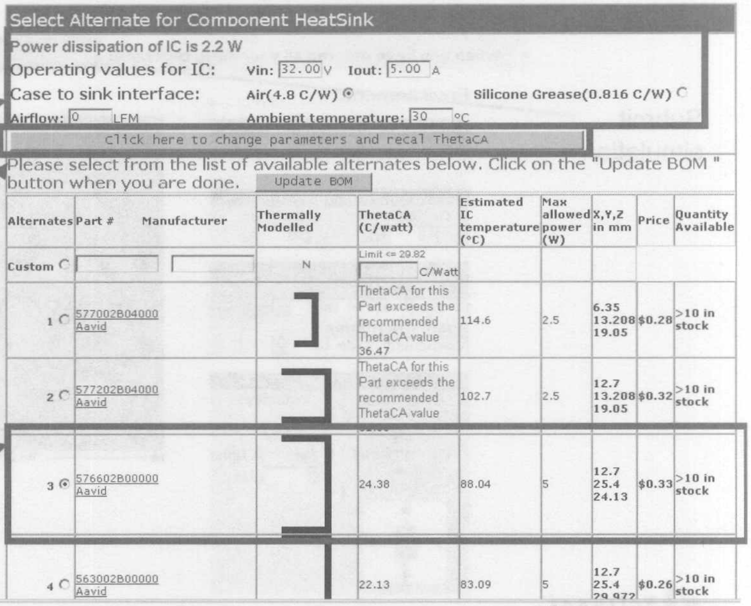
The thermal resistance for a package using a heat sink can be broken down into several components. This begins with the theta jc or thermal resistance from junction to case, for the package which is about 2.0 degrees C/W for a TO-220 type package. Next is the theta cs or thermal resistance from case to sink which is about .8 C/W for silicone grease and about 4.8 C/W for air. Lastly is the theta sa or thermal resistance from the sink to air which can range broadly depending on the design of the heat sink. The heat sink is also affected by the airflow: for natural convection (no fan), the power dissipation affects the theta sa. This is because as more power is dissipated, the part gets hotter and generates airflow around the heat sink due to the hot air rising. The input voltage and load current on the power supply are used in this case to determine the theta sa. For forced airflow, the air velocity determines the theta sa.

Change Heat Sink

Change environmental parameters affecting heat sink

Recalculate theta ca based on changed parameters

Select from list of heat sinks



Select Alternate for Component HeatSink

Power dissipation of IC is 2.2 W

Operating values for IC: Vin: 32.00 V Iout: 5.00 A

Case to sink interface: Air(4.8 C/W) ● Silicone Grease(0.816 C/W) ○

Airflow: 0 LFM Ambient temperature: 30 °C

Please select from the list of available alternates below. Click on the "Update BOM " button when you are done.

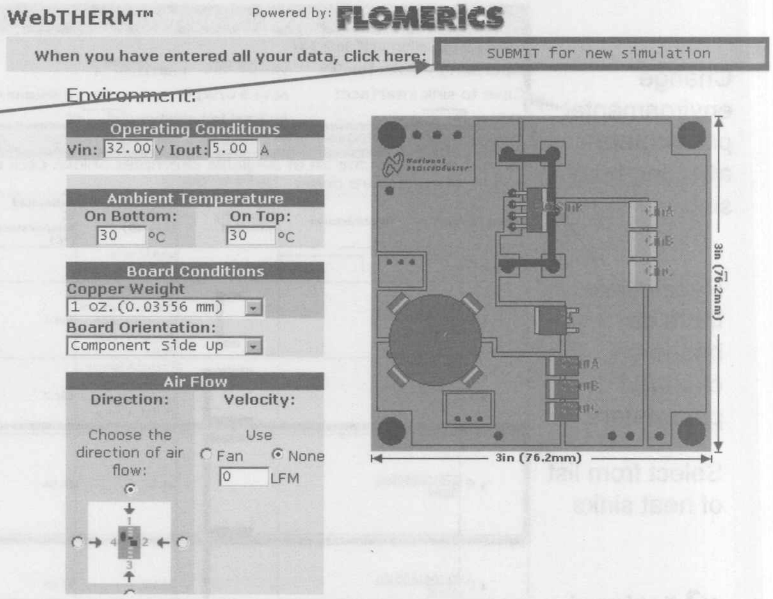
Alternates	Part #	Manufacturer	Thermally Modelled	ThetaCA (C/watt)	Estimated IC temperature (°C)	Max allowed power (W)	X,Y,Z in mm	Price	Quantity Available
Custom ○			N	Limit <= 29.82 C/Watt					
1 ○	577002B04000 Aavid			ThetaCA for this Part exceeds the recommended ThetaCA value 36.47	114.6	2.5	6.35 13.208 19.05	$0.28	>10 in stock
2 ○	577202B04000 Aavid			ThetaCA for this Part exceeds the recommended ThetaCA value	102.7	2.5	12.7 13.208 19.05	$0.32	>10 in stock
3 ●	576602B00000 Aavid			24.38	88.04	5	12.7 25.4 24.13	$0.33	>10 in stock
4 ○	563002B00000 Aavid			22.13	83.09	5	12.7 25.4 29.972	$0.26	>10 in stock

National Semiconductor

The Art of Analog 47

On this screen you enter the parameters affecting the heat sink. This includes the voltage and current which determine the power dissipation, the case to sink interface which can be air or grease, the airflow for forced convection if a fan is used, and the ambient temperature. After clicking on the "recal ThetaCA" button, the parameters for each heat sink will be recalculated. This makes it easy to select the best heat sink based on estimated IC temperature and cost. When you are finished selecting the heat sink, click on the "update BOM" button to save the choice and return to WebTHERM™.

Change Heat Sink



WebTHERM™

Powered by: FLOMERICS

When you have entered all your data, click here: SUBMIT for new simulation

Environment:

Operating Conditions

Vin: 32.00 V Iout: 5.00 A

Ambient Temperature

On Bottom: 30 °C

On Top: 30 °C

Board Conditions

Copper Weight: 1 oz.(0.03556 mm)

Board Orientation: Component Side Up

Air Flow

Direction: Choose the direction of air flow: ●

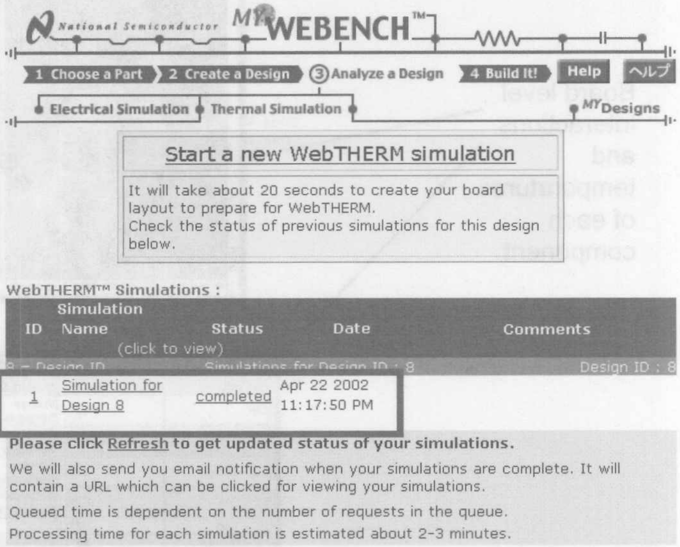
Velocity: Use ○ Fan ● None

0 LFM

Submit simulation

When we are finished entering the environmental information, click on the "SUBMIT" for new simulation button to begin the simulation.

Simulation Status Screen



Start a new WebTHERM simulation

It will take about 20 seconds to create your board layout to prepare for WebTHERM.
Check the status of previous simulations for this design below.

WebTHERM™ Simulations :

ID	Simulation Name (click to view)	Status	Date	Comments
8 – Design ID		Simulations for Design ID : 8		Design ID : 8
1	Simulation for Design 8	completed	Apr 22 2002 11:17:50 PM	

Please click Refresh to get updated status of your simulations.

We will also send you email notification when your simulations are complete. It will contain a URL which can be clicked for viewing your simulations.

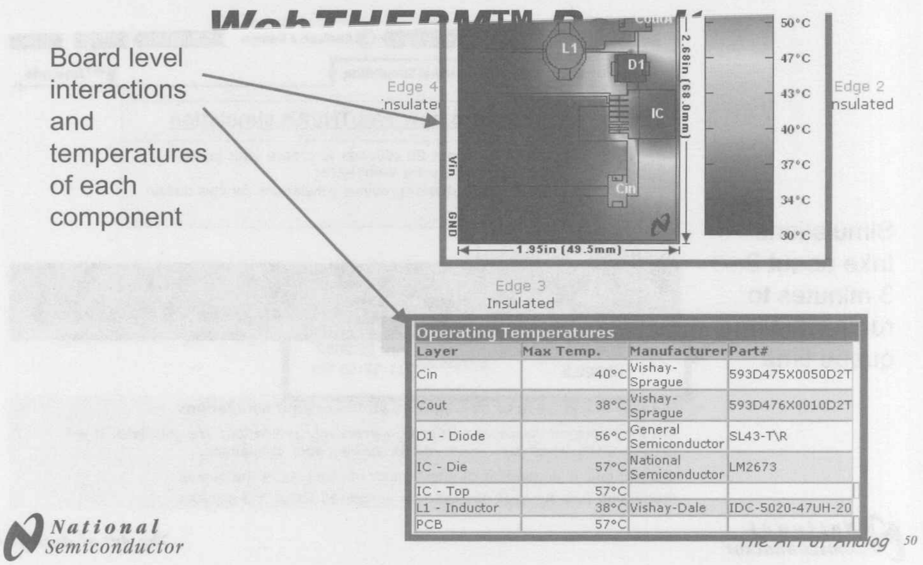
Queued time is dependent on the number of requests in the queue.

Processing time for each simulation is estimated about 2-3 minutes.

Simulations take about 2 – 3 minutes to run excluding queue time

National Semiconductor

All your simulations are listed on the simulation status screen. A simulation may be in queue, which means that it is waiting to start, in process, which normally takes about 2 to 3 minutes, or completed. To view a completed simulation, click on the link for the simulation, you can start a new simulation by clicking on the "Start a new WebTHERM™" simulation button. You can get back to this screen from anywhere in WebTHERM™ by clicking on the "Thermal Simulation" tab near the top center of the screen.

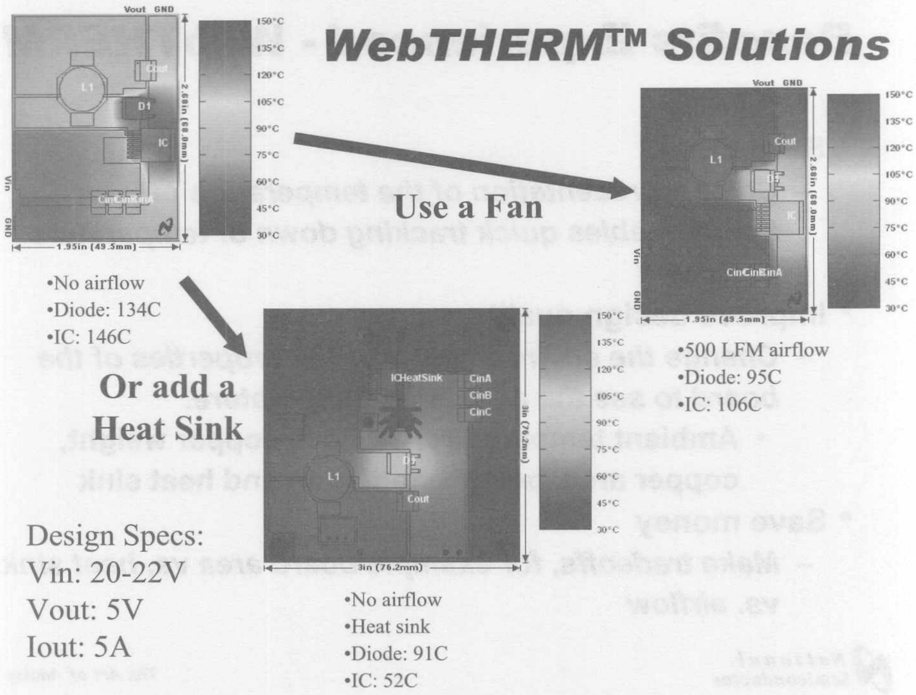


Board level interactions and temperatures of each component

Operating Temperatures

Layer	Max Temp.	Manufacturer	Part#
Cin	40°C	Vishay-Sprague	593D475X0050D2T
Cout	38°C	Vishay-Sprague	593D476X0010D2T
D1 - Diode	56°C	General Semiconductor	SL43-T\R
IC - Die	57°C	National Semiconductor	LM2673
IC - Top	57°C		
L1 - Inductor	38°C	Vishay-Dale	IDC-5020-47UH-20
PCB	57°C		

After about 2 to 3 minutes, depending on the complexity, the simulation is complete. The simulation results screen shows a color map of the temperatures across the PC board. It also indicates the temperature of each component. The plot can be rescaled to match other simulations, if desired. The user can go back and adjust the environmental variables or change the operating conditions of the design to improve the behavior if necessary. This can save a lot of time by reducing the number of iterations in the temperature lab.



WebTHERM™ Solutions

Use a Fan

- •No airflow
- •Diode: 134C
- •IC: 146C

- •500 LFM airflow
- •Diode: 95C
- •IC: 106C

Or add a Heat Sink

- •No airflow
- •Heat sink
- •Diode: 91C
- •IC: 52C

Design Specs:
Vin: 20-22V
Vout: 5V
Iout: 5A

Here is an example of how WebTHERM™ can be used to solve a temperature problem. We have created a power supply design with Vin ranging from 20 to 22 volts, Vout = 5 volts and Iout = 5 amps. With this high-current design, the components tend to get quite hot. In the first simulation, using no fan or heat sink, the regulator is over 140°C and the diode is over 130°C. We can add a fan with an air velocity of 500 linear feet per minute and the simulation shows that the temperature of the IC and diode drop to less than 110 degrees. However, the design is still too hot. Another approach is to add a heat sink which brings the temperature of the IC down to less than 60°C and the diode less than 100°C. Other possibilities are to increase the copper area or thicken the copper.

We are now done analyzing and optimizing our design and will proceed to the "Build It" step.

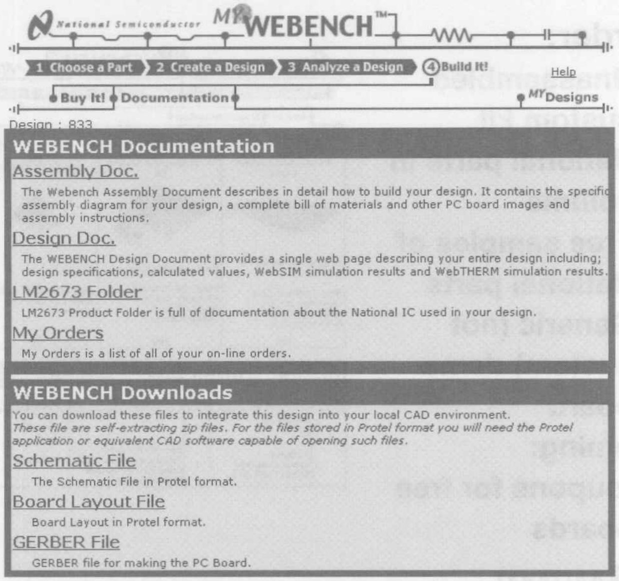
Benefits Experienced - WebTHERM

- Save time
  - *Color representation of the temperature of your board enables quick tracking down of temperature problems*
- Improve design quality
  - *Change the environment and the properties of the board to see the effects on temperature:*
    - Ambient temperature, air flow, copper weight, copper area, board orientation and heat sink
- Save money
  - *Make tradeoffs, for example board area vs. heat sink vs. airflow*

Design Documentation

Customized documentation

Download CAD files



Design : 833

WEBENCH Documentation

Assembly Doc.

The Webench Assembly Document describes in detail how to build your design. It contains the specifi assembly diagram for your design, a complete bill of materials and other PC board images and assembly instructions.

Design Doc.

The WEBENCH Design Document provides a single web page describing your entire design including; design specifications, calculated values, WebSIM simulation results and WebTHERM simulation results.

LM2673 Folder

LM2673 Product Folder is full of documentation about the National IC used in your design.

My Orders

My Orders is a list of all of your on-line orders.

WEBENCH Downloads

You can download these files to integrate this design into your local CAD environment.
These file are self-extracting zip files. For the files stored in Protel format you will need the Protel application or equivalent CAD software capable of opening such files.

Schematic File

The Schematic File in Protel format.

Board Layout File

Board Layout in Protel format.

GERBER File

GERBER file for making the PC Board.

We are now in the last step of the WEBENCH™ process, which is called "Build It". In the Documentation page of Build It, you can view customized documentation for your design. This starts with the assembly document which contains information for constructing your power supply, including an assembly diagram, schematic, bill of materials and instructions for building and testing the power supply.

From the Design Doc link you can also get full documentation of the design including the specifications, operating values and thermal simulation results.

A detailed summary of the integrated circuit with links to the datasheet and application notes is in the product folder.

My orders shows your custom power supply kit order status and history.

Downloadable schematic, layout and Gerber files are also available on this page. The schematic and layout files are in Protel format, so you must have Protel software or other software which can read the Protel file format to take advantage of these. The Gerber file is for the custom board used for this design.

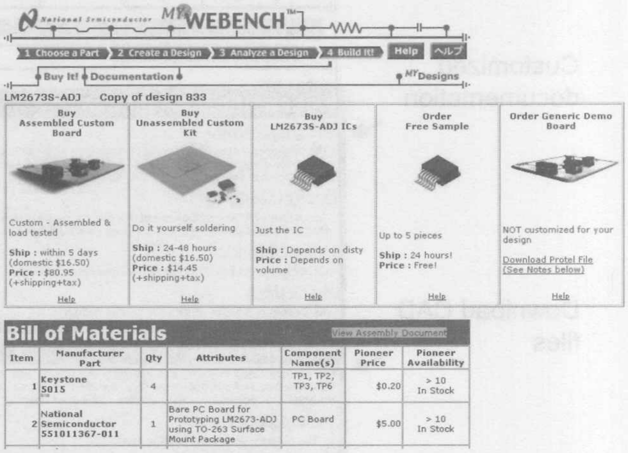
Build It

Order:

- **Unassembled custom kit**
- **National parts in volume**
- **Free samples of National parts**
- **Generic (not custom) demo board**

Coming:

Coupons for free boards



LM2673S-ADJ Copy of design 833

Buy Assembled Custom Board	Buy Unassembled Custom Kit	Buy LM2673S-ADJ ICs	Order Free Sample	Order Generic Demo Board
Custom - Assembled & load tested **Ship :** within 5 days (domestic $16.50) **Price :** $80.95 (+shipping+tax)	Do it yourself soldering **Ship :** 24-48 hours (domestic $16.50) **Price :** $14.45 (+shipping+tax)	Just the IC **Ship :** Depends on disty **Price :** Depends on volume	Up to 5 pieces **Ship :** 24 hours! **Price :** Free!	NOT customized for your design Download Protel File (See Notes below)

Bill of Materials

Item	Manufacturer Part	Qty	Attributes	Component Name(s)	Pioneer Price	Pioneer Availability
1	**Keystone 5015**	4		TP1, TP2, TP3, TP6	$0.20	> 10 In Stock
2	**National Semiconductor 551011367-011**	1	Bare PC Board for Prototyping LM2673-ADJ using TO-263 Surface Mount Package	PC Board	$5.00	> 10 In Stock

On the Buy It page of Build It you have a number of options to get your prototype quickly. Here you can get a custom kit for your design. This is sent to you within 2 days via overnight carrier. The kit has all the parts for your design which allows you to solder your prototype faster than ever. You can also order free samples of the National Semiconductor regulator (up to 5) or order larger quantities of the regulator. Lastly, if a generic demo board is available, you can order that. However the generic demo board is not customized to your design.

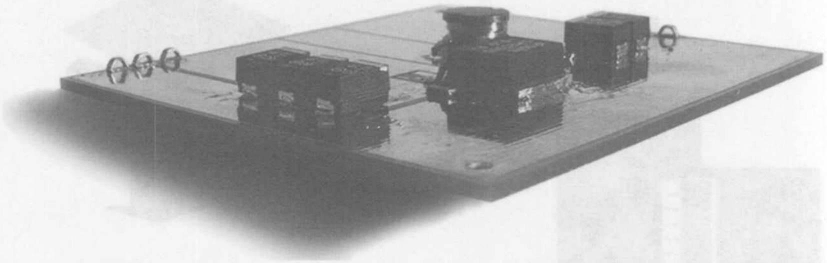
Benefits Experienced – Build It

- Save time
  - Get a Build It prototype kit overnight* or a fully assembled and tested board in 5 days*
  - Documentation automatically generated to support design, including board assembly notes and simulation summary,
  - Download schematic and layout files in Protel format and also Gerber files to incorporate the design directly into your CAD system
- Improve design quality
  - Confirm simulation results on the bench after obtaining Build It prototype
- Save money
  - Avoid costly board reworks and testing iterations

*If ordered before 1pm Eastern time to a US destination

- Reduce power supply design cycle time from weeks to hours using advanced Internet technology
- Improve design quality by optimizing design up front
- Save money by evaluating tradeoffs and options to achieve desired results in the most cost-effective manner

Your Prototype Power Supply



Faster Than Ever!

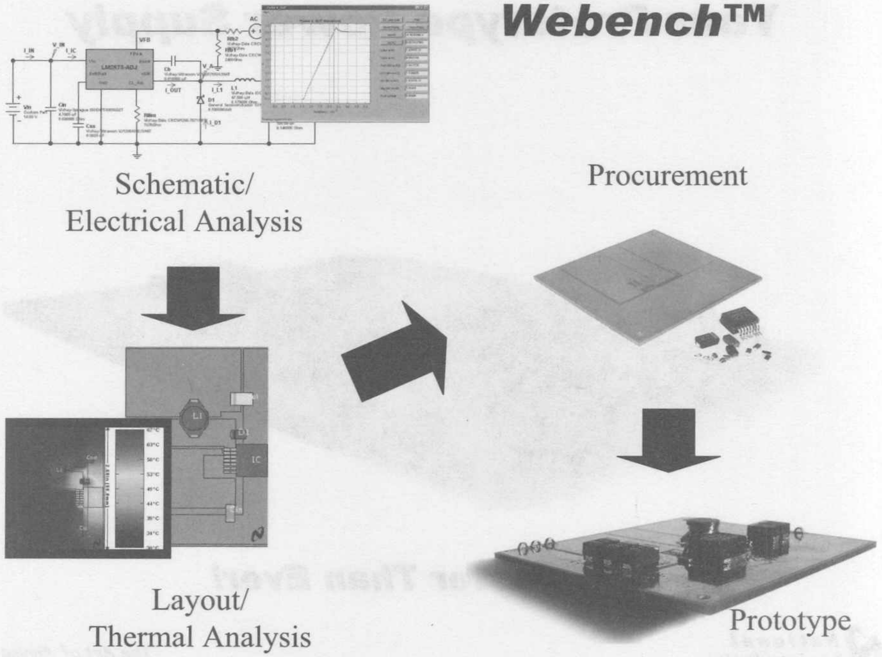
National Semiconductor

The Art of Analog 57

Following the assembly instructions from the web, you will be able to construct and test your prototype power supply board quickly and easily. Thus, you can see how WEBENCH™ saves you time and allows you to avoid costly mistakes by doing optimization up front in the design process, and then closes the loop by allowing you to to construct an actual prototype in record time.

WEBENCH redefines the way electrical design is done by using the power of the internet to save you time. Today, it is more important than ever for designers to get their products to market fast and WEBENCH fulfills that need by providing you with a complete start to finish solution.

Webench™



Schematic/
Electrical Analysis

Procurement

Layout/
Thermal Analysis

Prototype